

MANTIS_CML Schematic

2019/06/04

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Mantis_CML

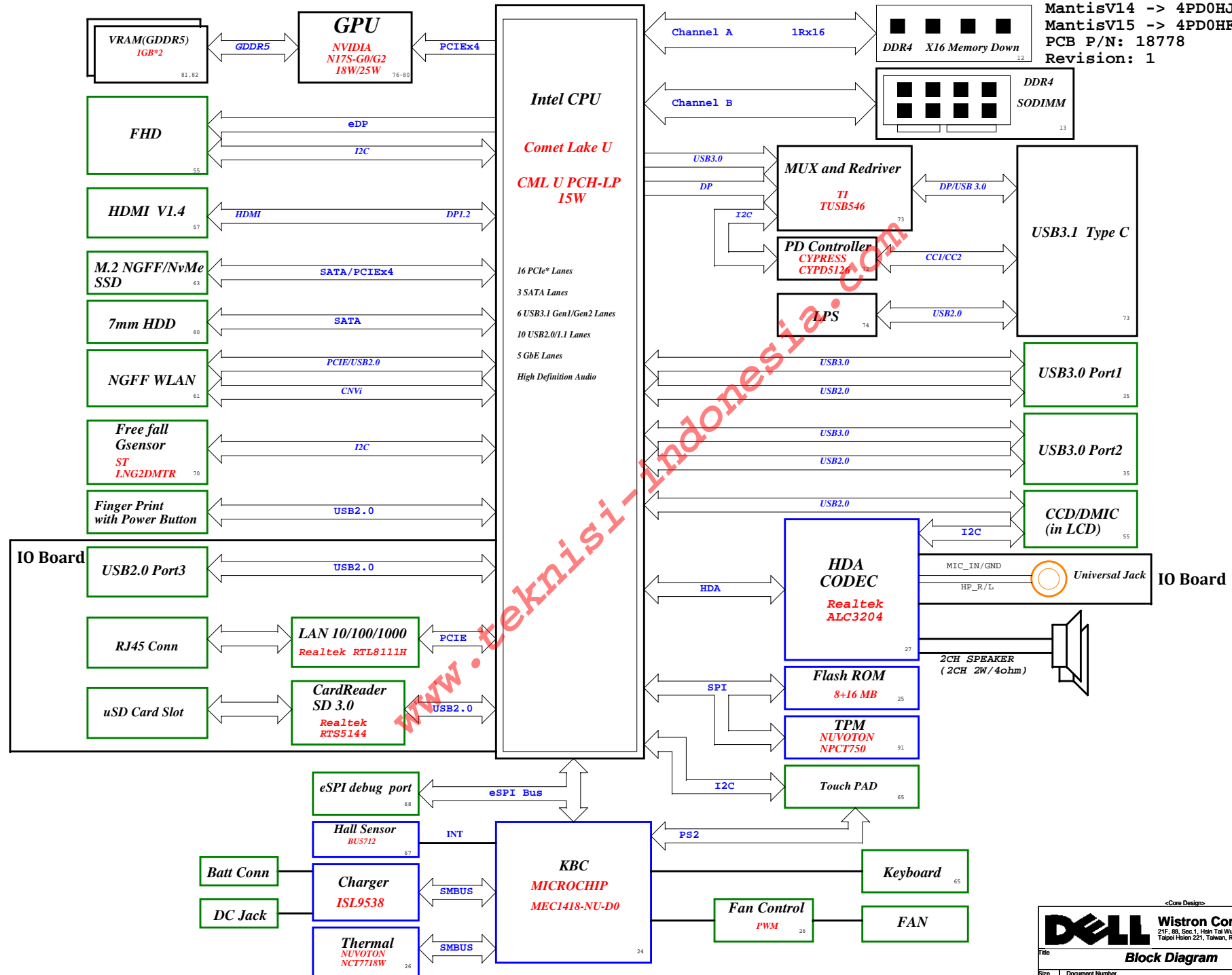
Rev
A00

Date: Monday, June 03, 2019

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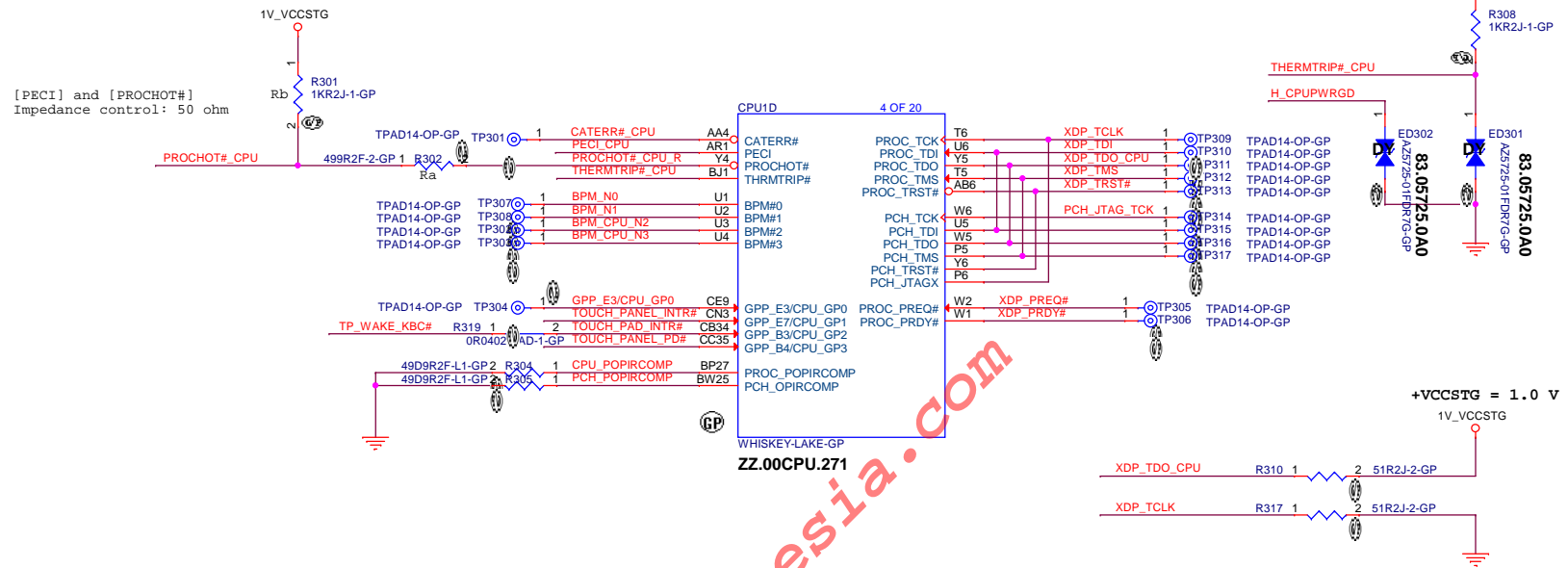
Mantis CML Block Diagram

Project code:
MantisN14 -> 4PD0HH010001
MantisN15 -> 4PD0HG010001
MantisV14 -> 4PD0HJ010001
MantisV15 -> 4PD0HF010001
PCB P/N: 18778
Revision: 1



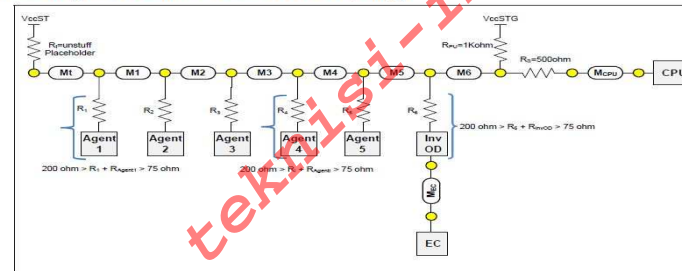
SSID = CPU

- [24] PECL_CPU <<>>
- [24,44,46] PROCHOT#_CPU <<>>
- [55] TOUCH_PANEL_INTR# <<<<
- [24,65] TP_WAKE_KBC# >>>>
- [17] H_CPUPWRGD >>>>
- [55] TOUCH_PANEL_PD# <<<<



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology

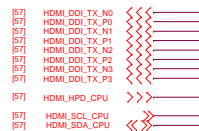


M1, 2, 3, 4, 5: < 4 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt < 0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

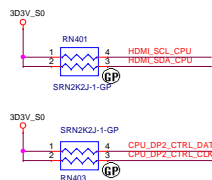
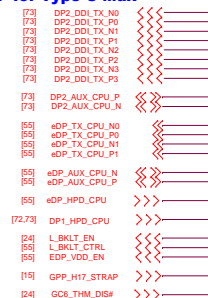
<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (THML/JTAG)			
Size: A3	Document Number:	Rev: A00	
Date: Tuesday, May 28, 2019		Sheet 3 of 105	

DP to HDMI2.0



DP for Type-C Mux



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

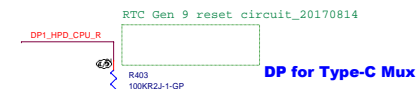
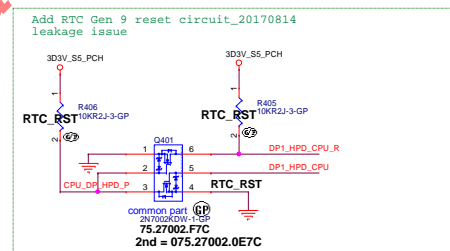
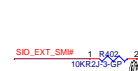
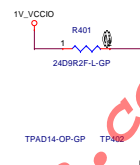
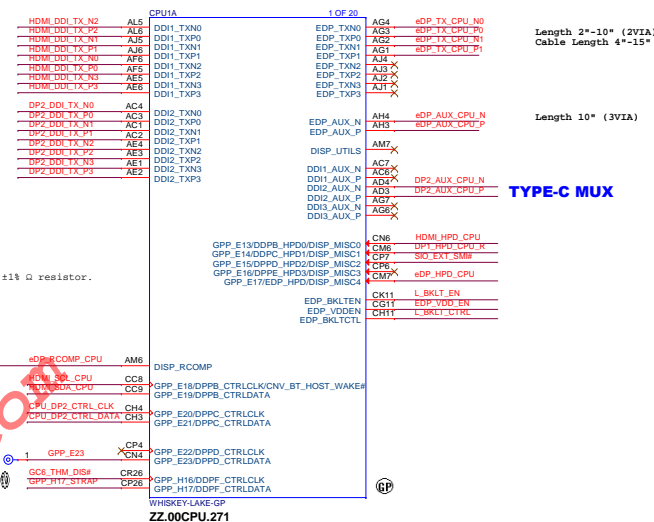
(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

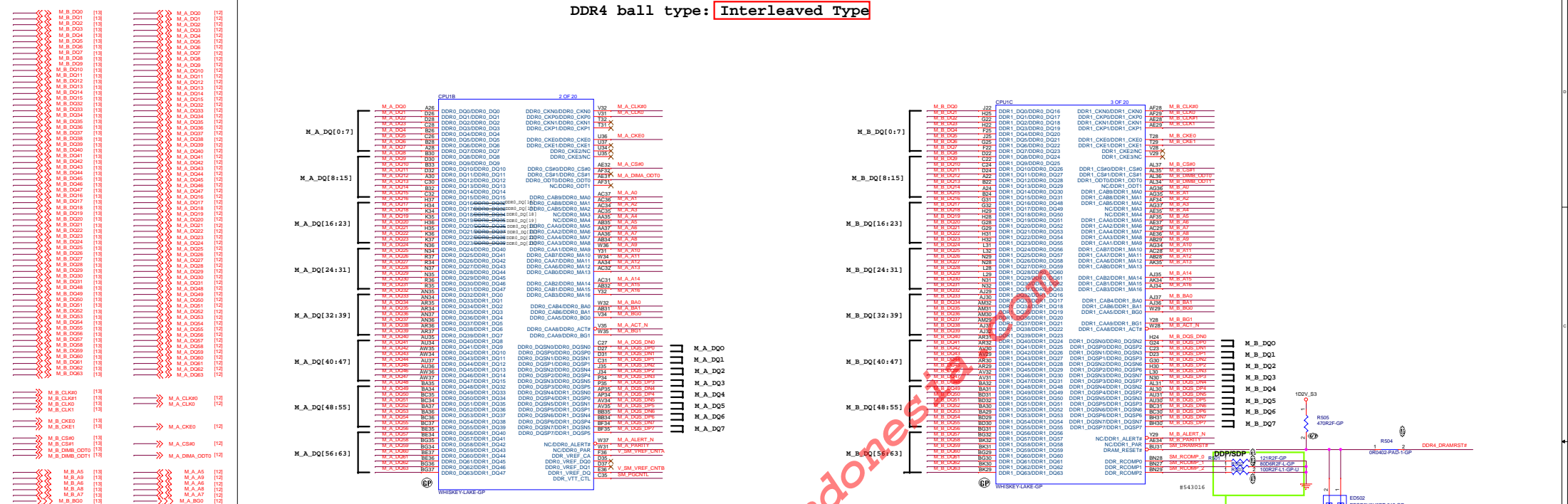
1.65GT Length 6.5" (3VIA)

DP to HDMI1.4b

DP for Type-C Mux



```
DDR4 ball type: Interleaved Type
```



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

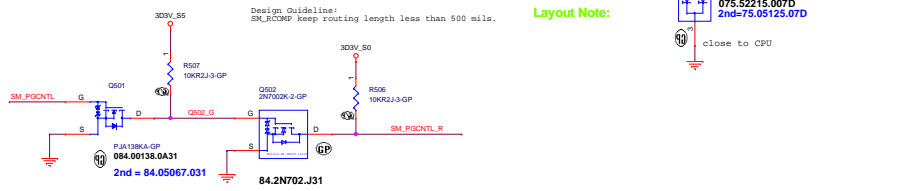
4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT, Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1's ODT not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

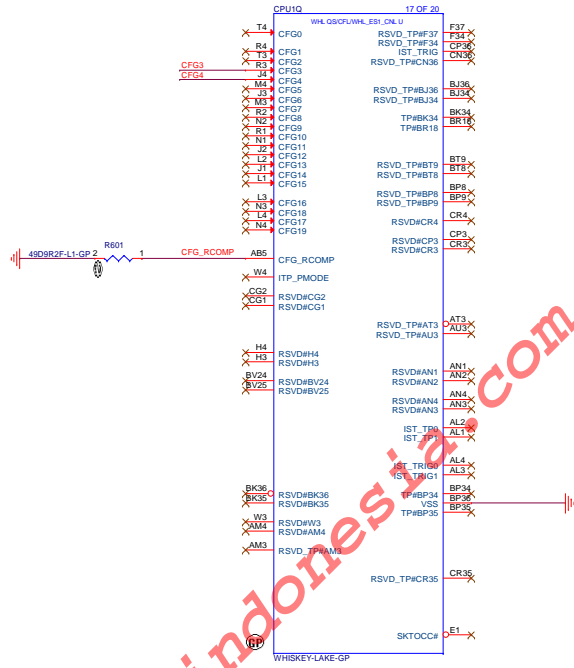
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



Layout Note:

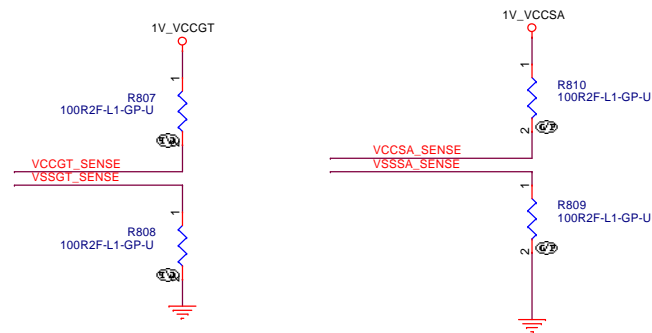
SSID = CPU

[19] CFG3 <<< _____
[19] CFG4 <<< _____



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

Pin Number	CFI-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCORE
AB10	VCCGT	VCCGT	VCCORE
AB2	VCCGT	VCCGT	VCCORE
AB8	VCCGT	VCCGT	VCCORE
AB9	VCCGT	VCCGT	VCCORE
AC8	VCCGT	VCCGT	VCCORE
AD9	VCCGT	VCCGT	VCCORE
AE10	VCCGT	VCCGT	VCCORE
AE8	VCCGT	VCCGT	VCCORE
AE9	VCCGT	VCCGT	VCCORE
AF10	VCCGT	VCCGT	VCCORE
AF2	VCCGT	VCCGT	VCCORE
AF8	VCCGT	VCCGT	VCCORE
AG8	VCCGT	VCCGT	VCCORE
AG9	VCCGT	VCCGT	VCCORE
AH9	VCCGT	VCCGT	VCCORE
AJ10	VCCGT	VCCGT	VCCORE
AJ8	VCCGT	VCCGT	VCCORE
AK2	VCCGT	VCCGT	VCCORE
AK9	VCCGT	VCCGT	VCCORE
AL10	VCCGT	VCCGT	VCCORE
AL8	VCCGT	VCCGT	VCCORE
AL9	VCCGT	VCCGT	VCCORE
AM8	VCCGT	VCCGT	VCCORE
V2	VCCGT	VCCGT	VCCORE
Y10	VCCGT	VCCGT	VCCORE
Y8	VCCGT	VCCGT	VCCORE



Main Func = CPU

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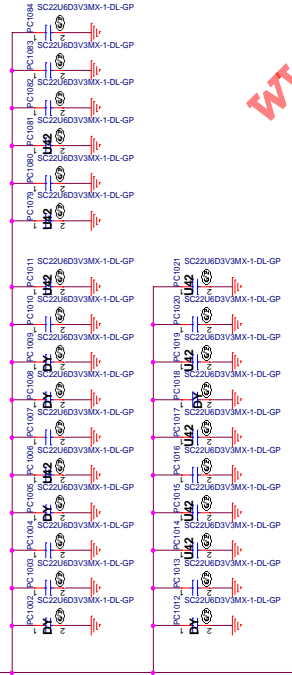
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (RSVD)		
Size	Document Number				Rev
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1V_CPU_CORE

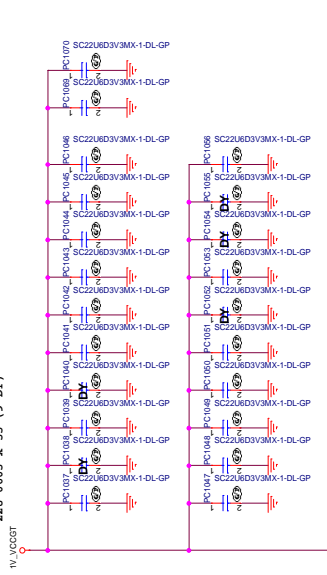
1V_CPU_CORE

220 0603 x 39 (7DY)



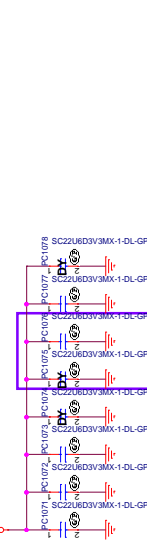
VCCGT

220 0603 x 35 (9 DY)



VCCSA

220 0603 x 8 (3DY)



X02 20190412

Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCGT	15x 22uF 0603 4x 47uF 0805 (6.3V)		Place underneath the package
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
VCCSA		4x 0402	Placeholder only.
	6x 10uF 0402	7x 10uF 0402	
	2x 47uF 0805 (6.3V)		
VCCGT	2x 0805	4x 1uF 0402/0201	Place as close to the package as possible.
	1x 22uF 0603	3x 10uF 0402	
VCCGT	6x 10uF 0402	4x 1uF 0201	Place underneath the package
	4x 1uF 0402	6x 10uF 0402	Place as close to the package as possible
VCCGT	4x 0402		Placeholder Only
VCCGT	1x 1uF 0402		Do not merge VCCGT, VCCGT, and VCCGT to any noisy and high current power rail and do not route them close to the power rail. The power rail should be routed on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCGT	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or back side cap.
VCCGT	1x 0805		Placeholder Only.
VCCGT	1x 1uF 0402		Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		

Notes:

- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a 6.3V voltage.
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

Core Design

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21F, 4B, Sec. 1, Hsin Tsing Rd., Hsinchu,
Taiwan 300, R.O.C.

CPU(CORE Power Cap1)

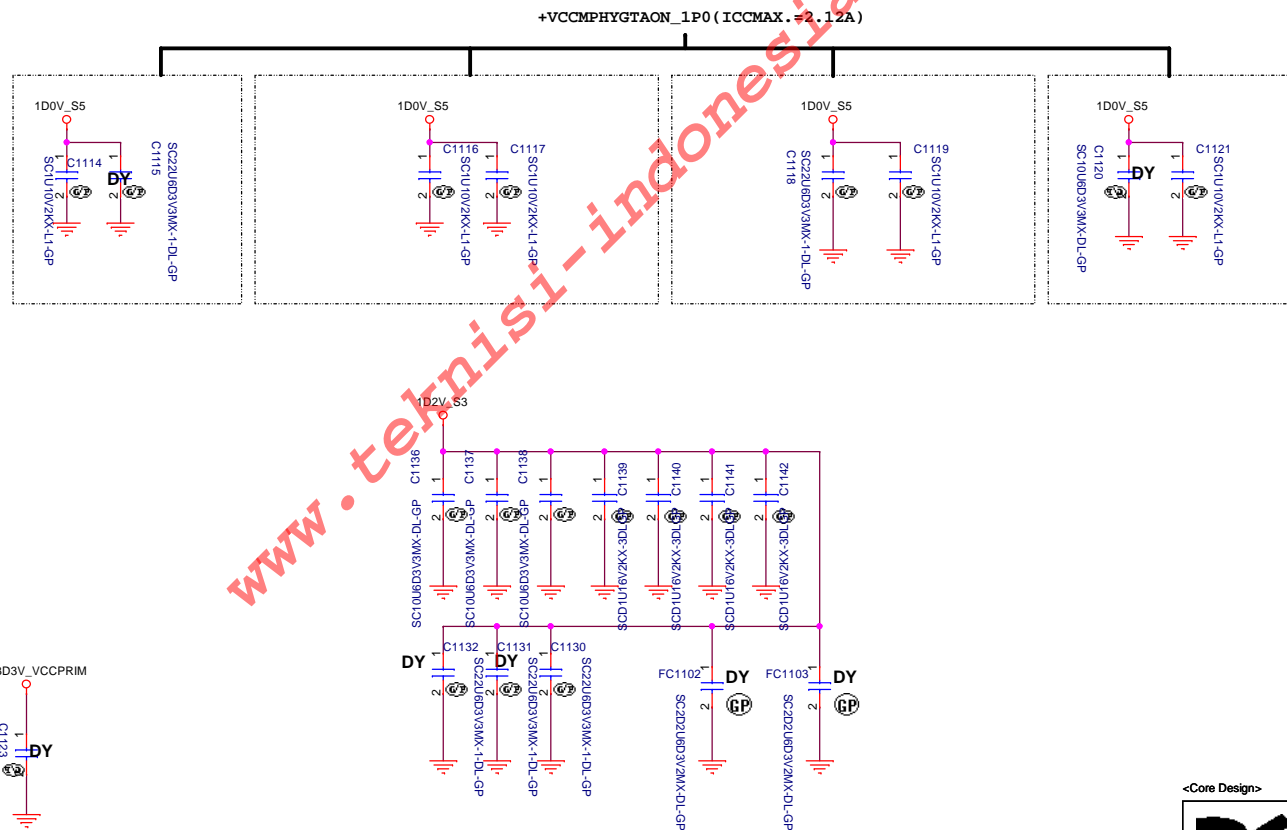
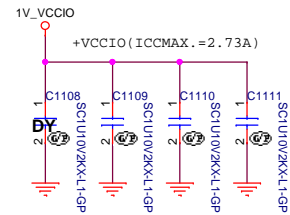
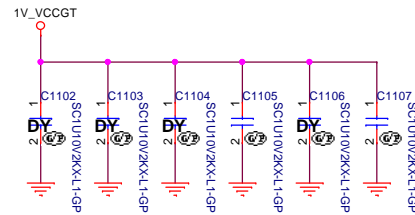
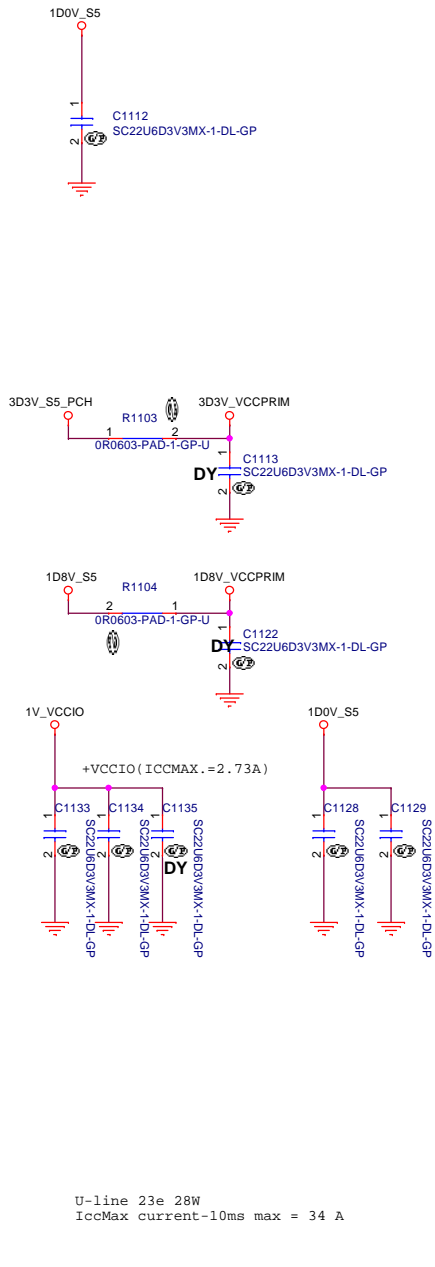
Rev. A
Document Number
Minds CML
Date: 08/07/2019
Page: 10

SSID = CPU

PCH DERIVED RAILS

UNSLICED GT

VCCIO



Layout Note:

1uF:

- C1174 near N15
- C1180 near K15
- C1173 near AF20
- C1172 near N18
- C1175 near AB19

22uF :

- C1182 C1184 near N15

10uF:

- C1176 near N15

<Core Design>

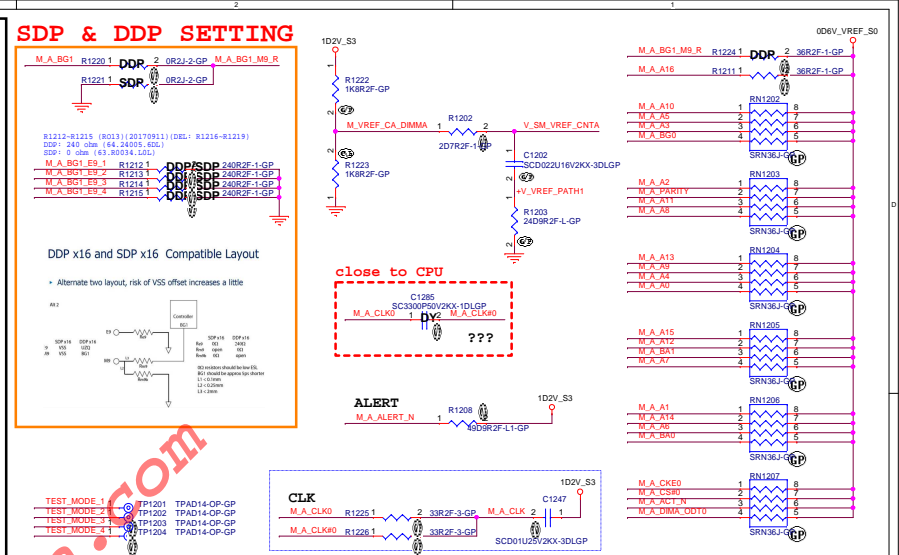
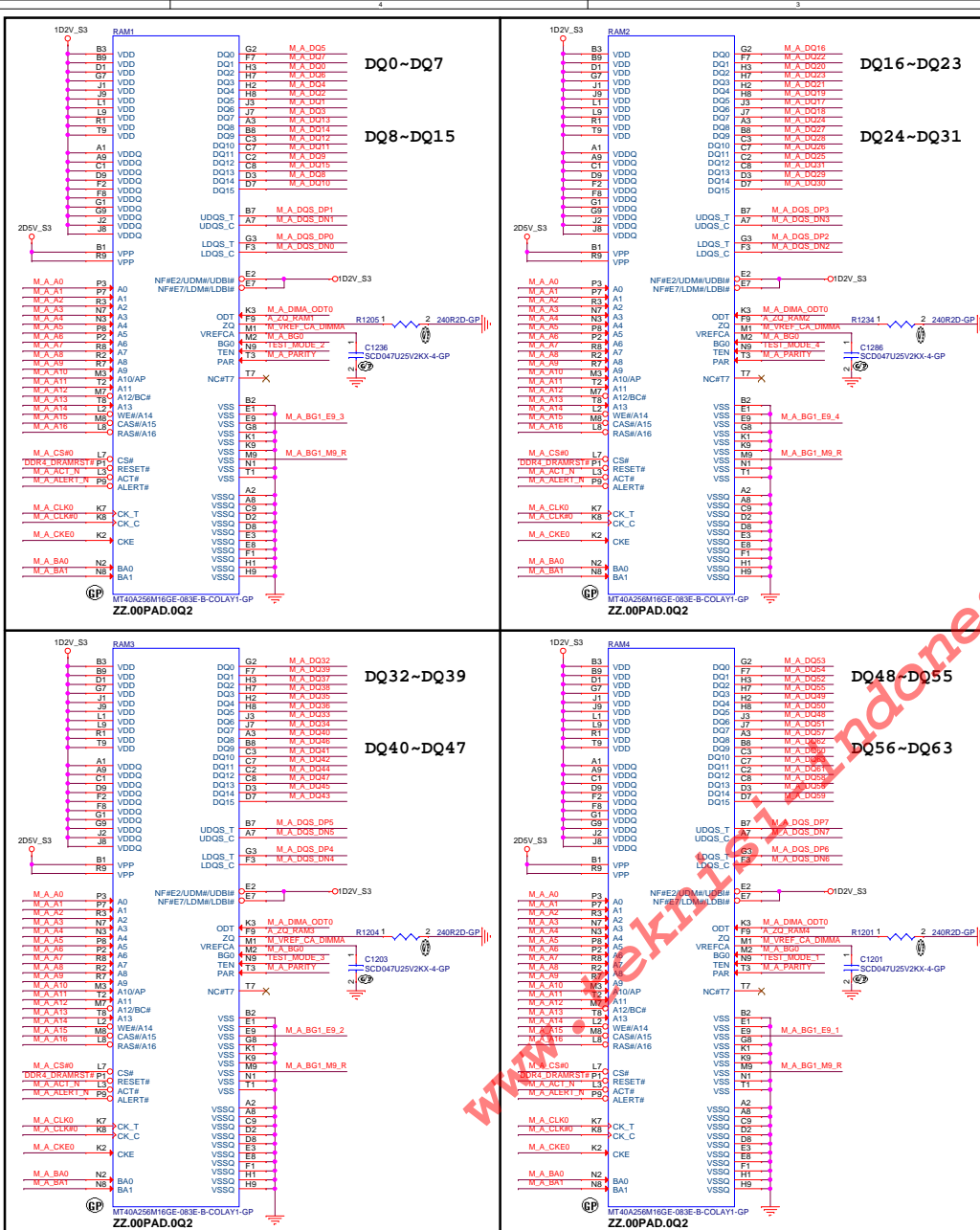
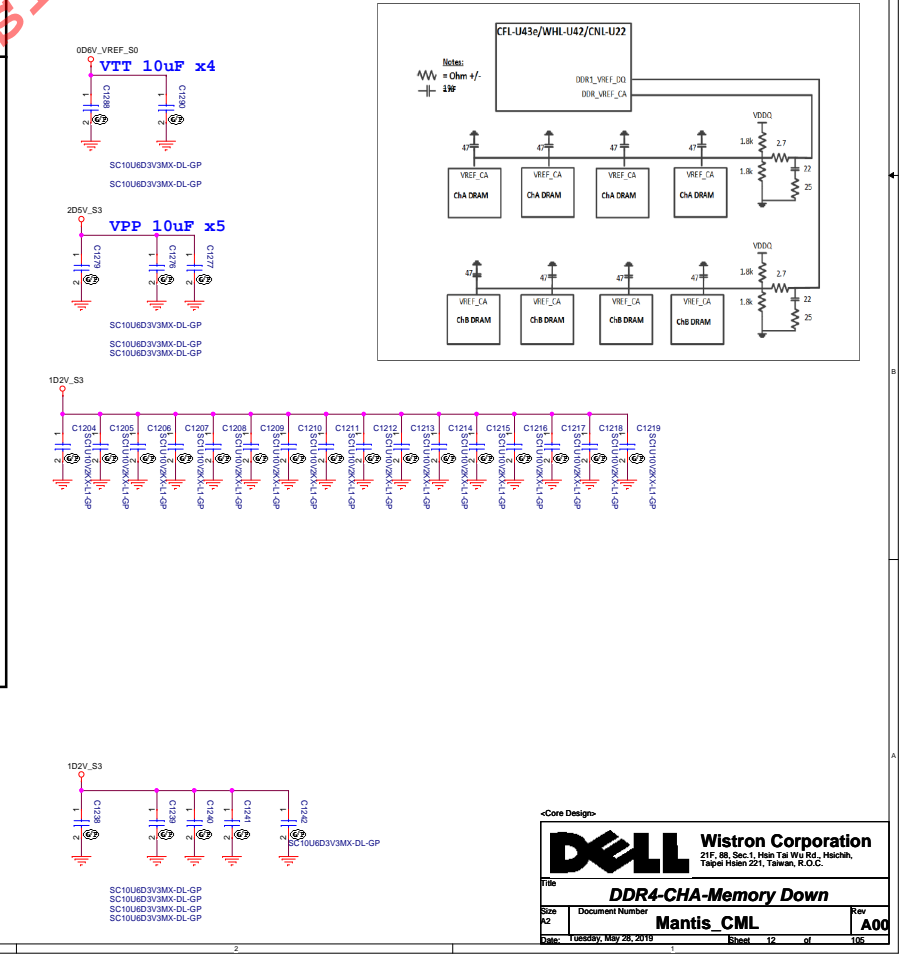
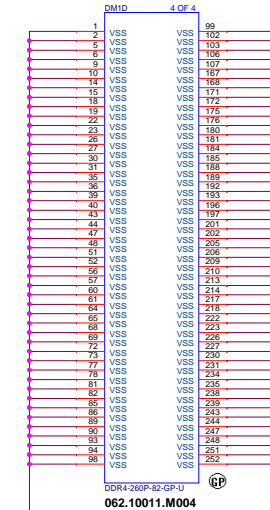
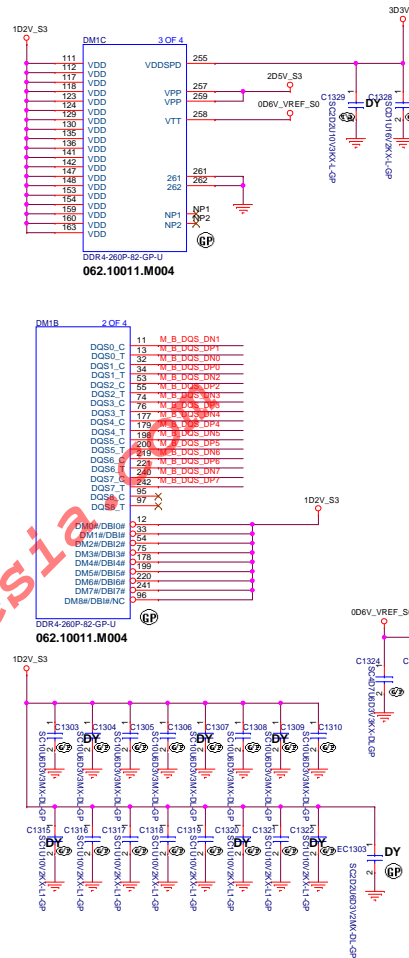
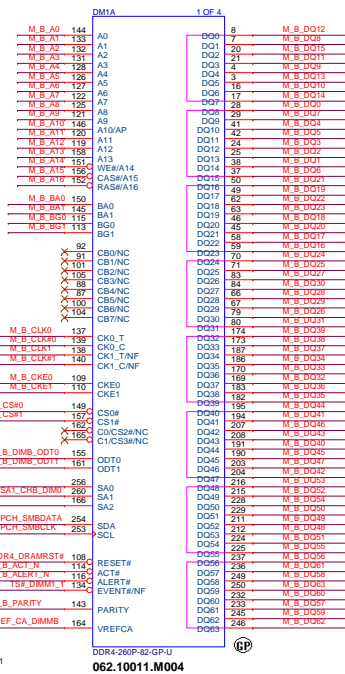
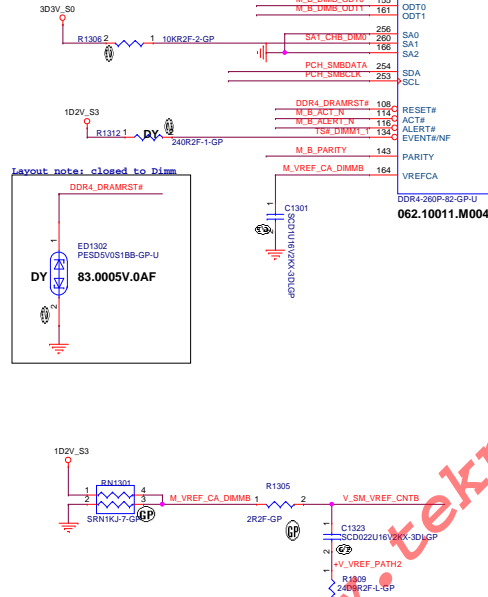


Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview






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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title DDR (RSVD) (DDR4-CHA1)		
Size A4	Document Number Mantis_CML	Rev A00
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CPU_SMB_ALERT4_F1

Page 4 86455 2.26.00 3.30.00

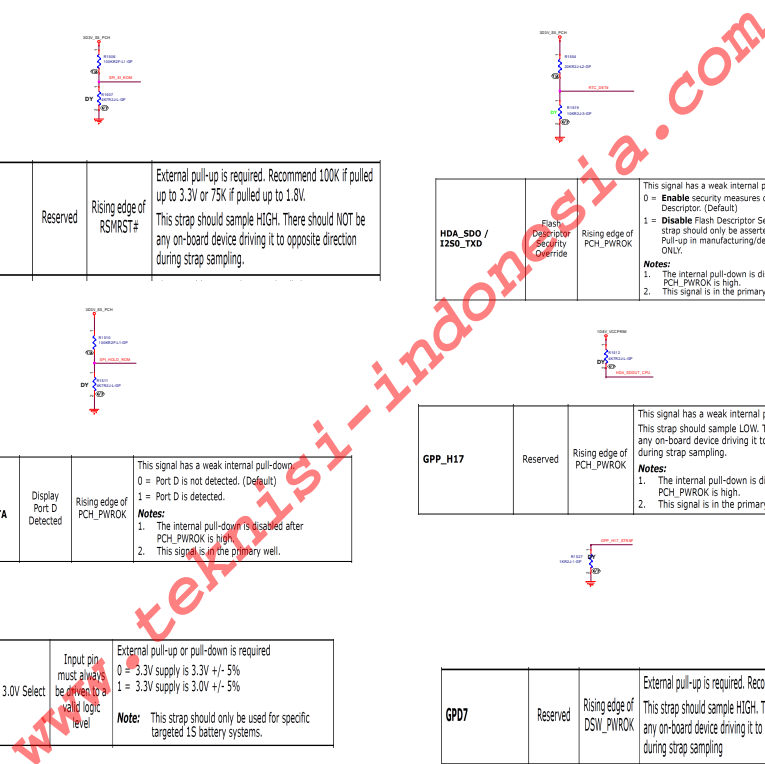
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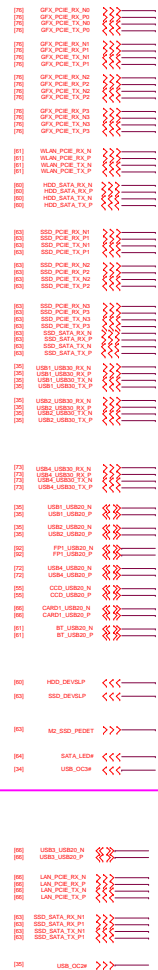
TABLE 2. PHYSICAL PROPERTIES

OFF_#23

TABLE 2. PHYSICAL PROPERTIES

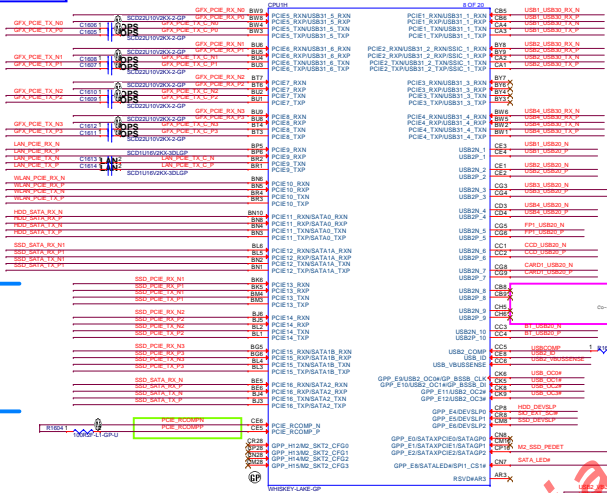
OFF_#23





#5430161:
220 nF nominal capacitors are recommended for Gen 1.
100 nF nominal capacitors are recommended for Gen 2.

GPU
LAN
WLAN
HDD1
SSD
Celeron CPU only
SSD



Layout Note:

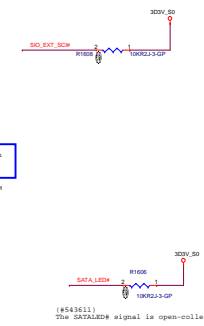
- 1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
- Note: Must maintain low DC resistance routing (<0.1 ohm).
- 2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

#545659 The xHCI controller supports USB Debug port on all USB3.0 capable ports.

- USB3 (USB3.0 Port1)
- USB4 (USB3.0 Port2)
- USB3.0 Type C
- USB3 (USB3.0 port1)
- USB4 (USB3.0 port2)
- USB2 (USB2.0 Port3 on IOBD)
- USB3.0 Type C
- Finger Print (USB2.0 Port5)
- CAMERA (USB2.0 Port6)
- Card Reader (USB2.0 Port7)

Bluetooth (USB2.0 Port10)

#545659: Must be used as DEVSLP, no external pull-up or pull-down termination required from DATA Host DEVSLP.



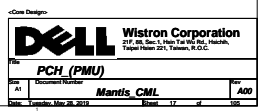
USB Type	Manufacturer	Model
USB3.0	Intel	Intel USB3.0
USB3.0	Intel	Intel USB3.0
USB3.0	Intel	Intel USB3.0
USB3.0	Intel	Intel USB3.0

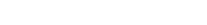
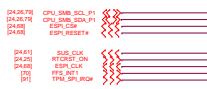
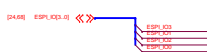
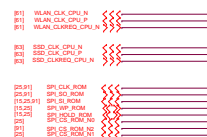
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

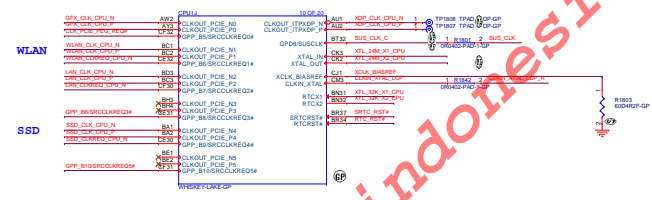
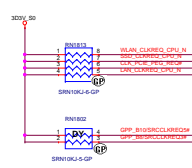
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	CBE	CBE	CBE	SATA 0	SATA 1,5	CBE	CBE	CBE	CBE	SATA 2	
Intel® RST Support	No Support					No Support			Yes			Yes					

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
		Cycle Router #1				Cycle Router #2				Cycle Router #3				Cycle Router #4			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP3				RP7				RP11				RP15			
	2x2	RP1	RP2	RP3	RP4	RP5	RP7	RP8	RP9	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18
	2x1+2x1	RP4	RP3	RP1	RP5	RP6	RP7	RP8	RP9	RP11	RP11	RP5	RP13	RP15	RP13	RP16	RP18
	2x1+2x1	RP4	RP3	RP1	RP5	RP6	RP7	RP8	RP9	RP11	RP11	RP5	RP13	RP15	RP13	RP16	RP18
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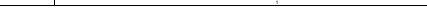
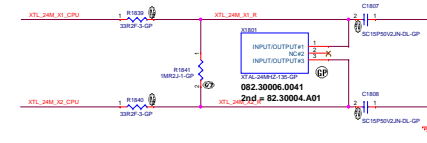
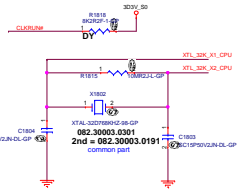
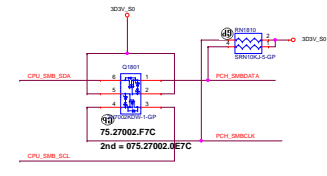
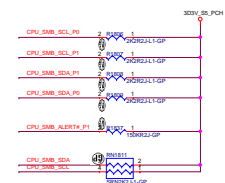
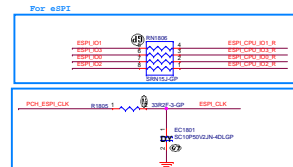




Frequency to Avoid: 33 MHz

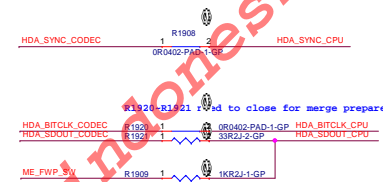
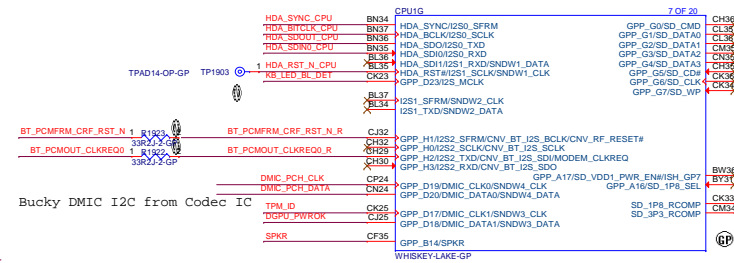
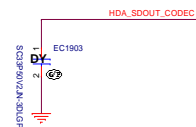
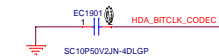
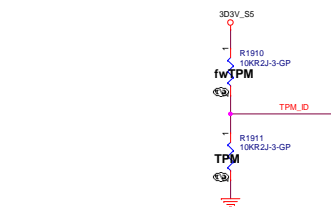
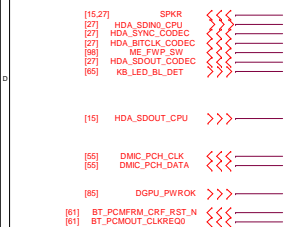


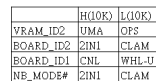
SSID



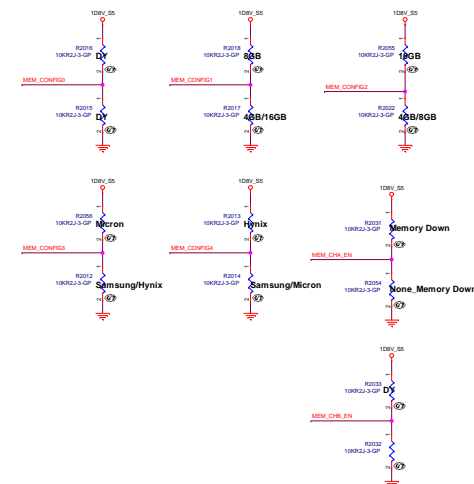
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SSID = PCH

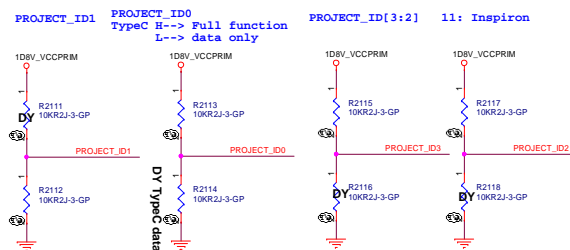
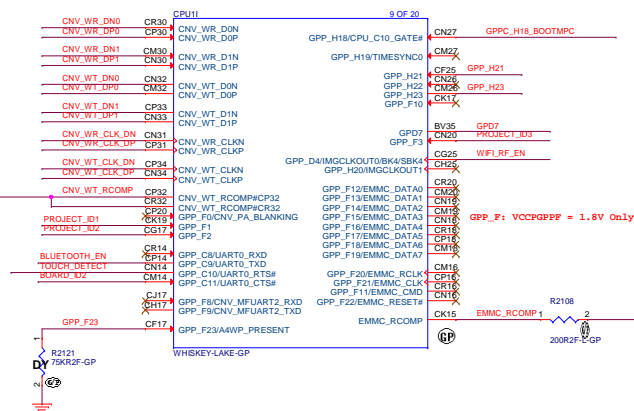
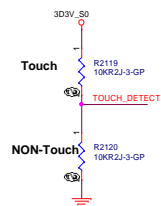




Vendor	MEM_CONFIG[0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron P/N	Capacity
Hynix	NA	00	01	H5AN8GNCNR-KVC	WDFJWSBA	4GB
Micron	NA	00	10	MT4AS12M16LY-075-E	WDFJWSCA	4GB
Samsung	NA	00	00	K4AAG16SWC-BCTD	WDFJWSAA	4GB
Hynix	NA	01	01	H5ANAGNCMR-KVC	6K9H9SBA	8GB
Micron	NA	10	10	MT40A1G16KNR-075-E	6K9H9SCA	8GB
Samsung	NA	10	00	K4AAG16SWB-MCTD	6K9H9SAA	8GB



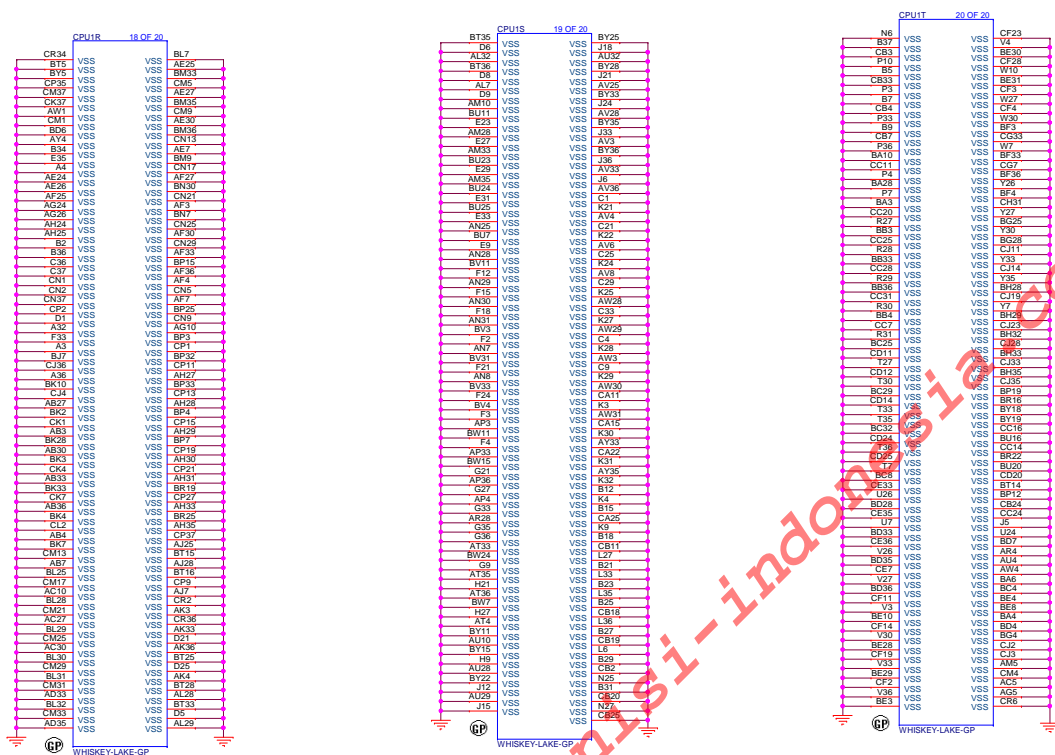
SSID = PCH



	H(10K)	L(10K)	Note
PROJECT ID0	TypeC full	TypeC data	TypeC function det
PROJECT ID1	Non	Non	follow Rogue define
PROJECT ID2	Non	Non	
PROJECT ID3	Non	Non	



1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of R(un)way, and E(dge) decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement.
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.




Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A1
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	Corner A71

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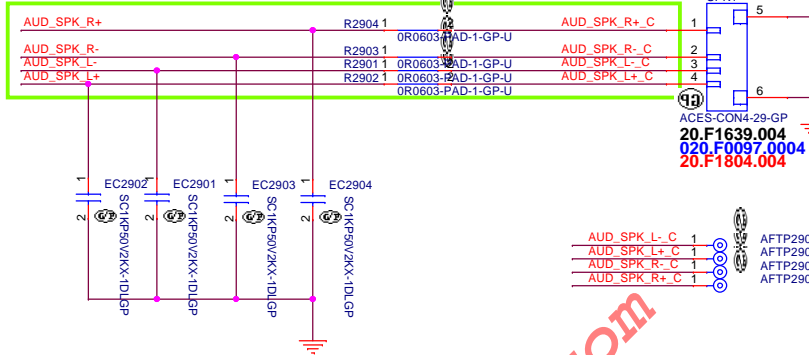
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Mantis_CML		Rev A00
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Main Func = Audio

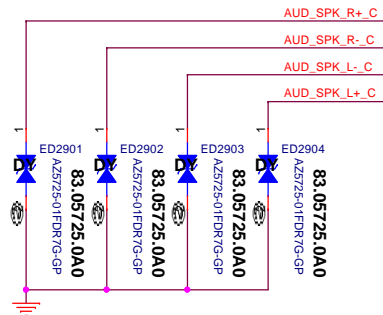
[27] AUD_SPK_R+ >>> _____
[27] AUD_SPK_R- >>> _____
[27] AUD_SPK_L- >>> _____
[27] AUD_SPK_L+ >>> _____

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

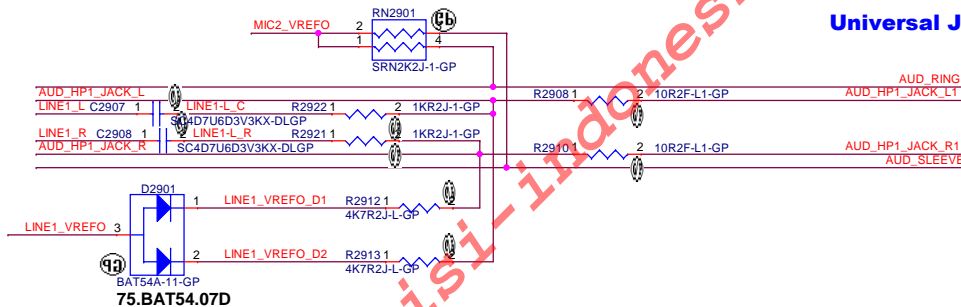


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L-
Pin4	SPK_L+



From Codec

[27] MIC2_VREFO >>> _____
[27,29,66] AUD_RING <<< _____
[27] AUD_HP1_JACK_L >>> _____
[27] LINE1_L >>> _____
[27] LINE1_R >>> _____
[27] AUD_HP1_JACK_R >>> _____
[27,29,66] AUD_SLEEVE <<< _____
[27] LINE1_VREFO >>> _____



Universal Jack (Moved to I/O Board)

To IO Board

[27,29,66] AUD_RING <<< _____
[66] AUD_HP1_JACK_L1 <<< _____
[66] AUD_HP1_JACK_R1 <<< _____
[27,29,66] AUD_SLEEVE <<< _____

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Main Func = LAN

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Title

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Size

Document Number

Rev

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Mantis CML

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Main Func = LAN

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Title

XFOM&RJ45

Size
A3

Document Number
Mantis_CML

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A00

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Main Func = Card Reader

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Title

Card Reader-RTS5170

Size
A4

Document Number
Mantis_CML

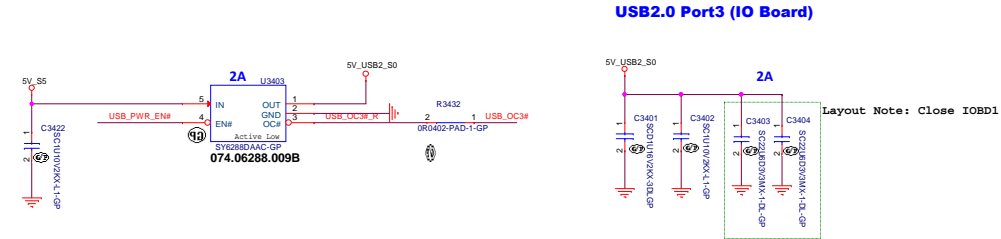
Rev
A00

Date: Tuesday, May 28, 2019

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Main Func = USB2.0

[16] USB_OC# <<<
[24,35] USB_PWR_EN# >>>



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Main Func = USB3.0 Port1

[P434] USB_PWR_ENW >>>

[1M] USB_OCIN <<<

[1M] USB1_USB30_N <<<

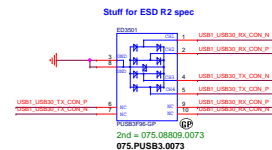
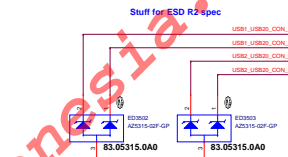
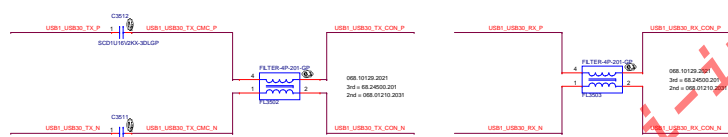
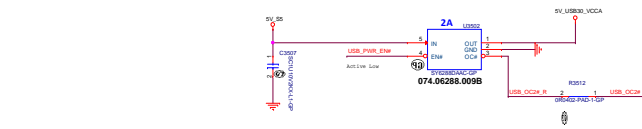
[1M] USB1_USB30_P <<<

[1M] USB1_USB30_TX_N >>>

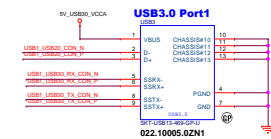
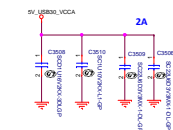
[1M] USB1_USB30_TX_P >>>

[1M] USB1_USB30_RX_N >>>

[1M] USB1_USB30_RX_P >>>



USB3.0 Port 1 Layout Note: Close USB3



Main Func = USB3.0 Port2

[1M] USB2_USB30_N <<<

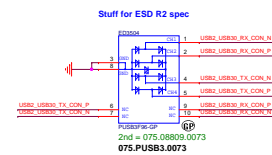
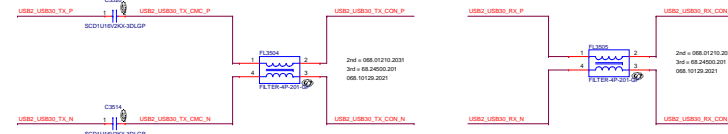
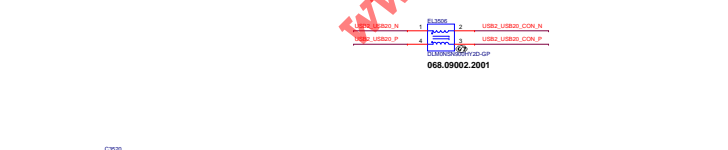
[1M] USB2_USB30_P <<<

[1M] USB2_USB30_TX_N >>>

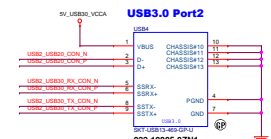
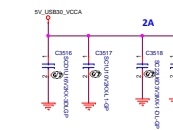
[1M] USB2_USB30_TX_P >>>

[1M] USB2_USB30_RX_N >>>

[1M] USB2_USB30_RX_P >>>




USB3.0 Port 2 Layout Note: Close USB4



Main Func = USB Charger

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Title

USB Charger


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<Core Design>

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Title		
USB3.0 PORT		
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5V_S0 & 3D3V_S0

[17.27] PM_SLP_S4 >>>
[17.24.26] RESET_OUT1 >>>

HW_SHUTDOWN

[46] 3V_S0_EN <<<
[38] PURE_HW_SHUTDOWN >>>
[34] ALVON >>>

POWER GOOD

[31] 102V_VTT_PWRGD >>>

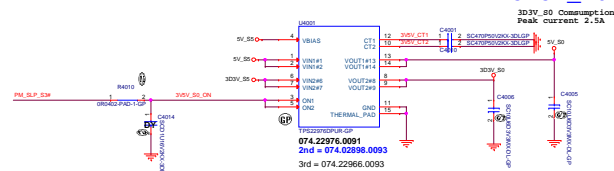
VCCIO & VCCSTG

[39] 102V_S0_PWRGD >>>
[4.53] P8B_PWRGD >>>

[31] GPMC_H18_BOOTMPC <<<

[17.24.48] VCCST_PWRGD <<<

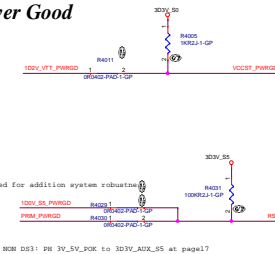
ROSA Run Power



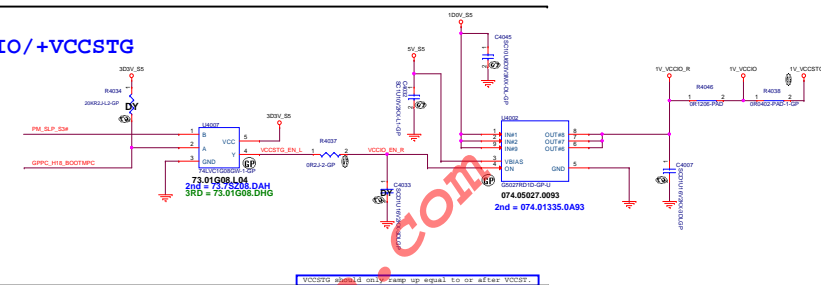
ROSA Run Power

074.22976.0091
2nd = 074.02898.0093
3rd = 074.22966.0093

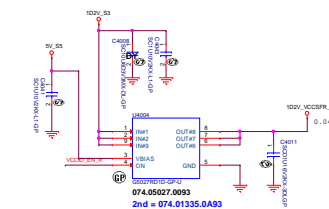
Power Good



+VCCIO/+VCCSTG



1D2V_VCCSFR_OC



MANAGEMENT RAIL POWER GENERATION

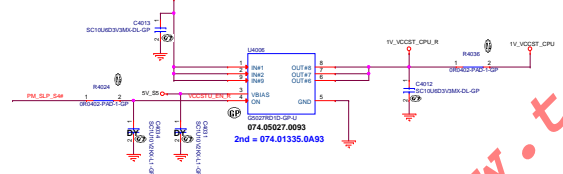
VCCST, VCCSTG, and VCCSTL can remain powered during S4 and S5 power states for board VB optimisation.

VCCST_CPU

VCCST_CPU

[17.31.32] PM_SLP_S4 >>>


VCCST_CPU



Main Func = Power & Sequence

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Title Connected_Standby(1/2)+DS3		
Size A4	Document Number Mantis_CML	Rev A00
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(2/2)		
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Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

DCR=0.02 ohm
Max current = 6000mA

624.00AM

and

ACN7403-
84.0740

Barrel Adapter Plug-in Detect

Main Func = M-BAT Input

Batt Connector

Placement: Close to Batt Connector

2nd = 75.00099.K70

3rd = 75.00099.Q7D
4th = 75.00099.D7D

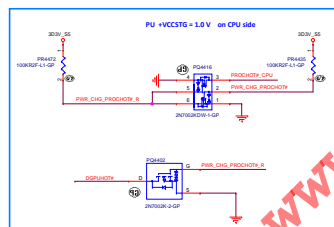
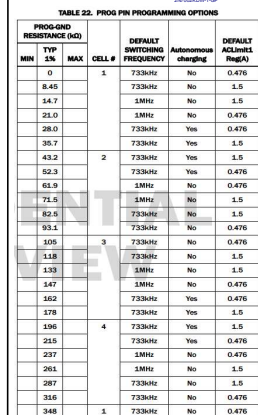
491 = 73.000995.D7D

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File _____			
Size _____		DCIN Mantis CML	
At _____	Document Number _____	Know _____	Know _____
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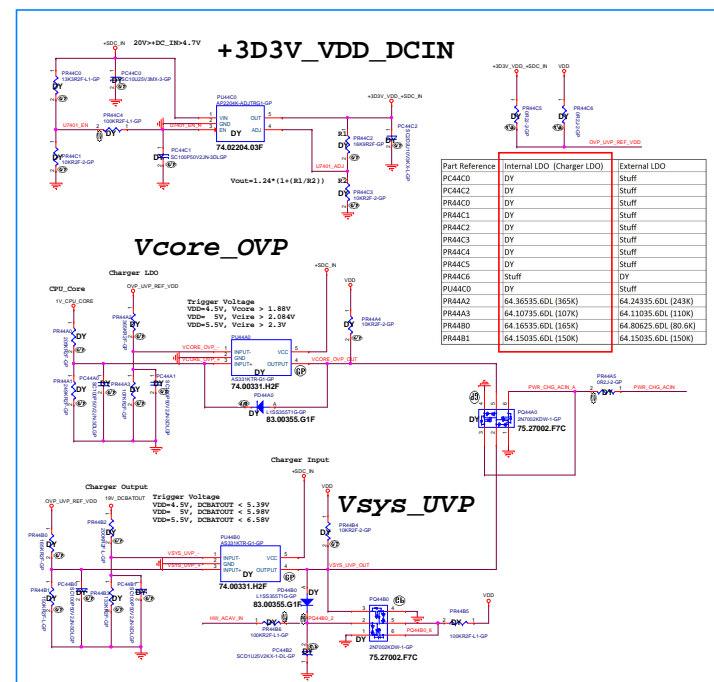
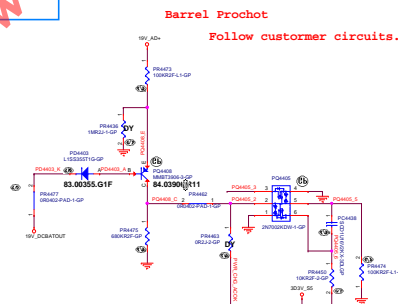
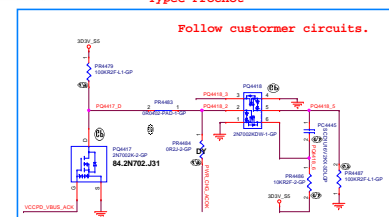
20

EE needs check it!!



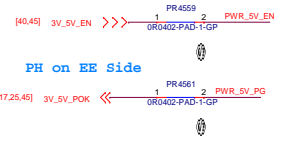
TypeC Prochot

Follow customer circuits.

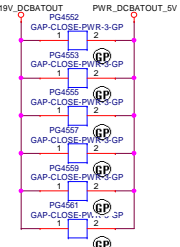


SSID = PWR.Plane.Regulator_5V

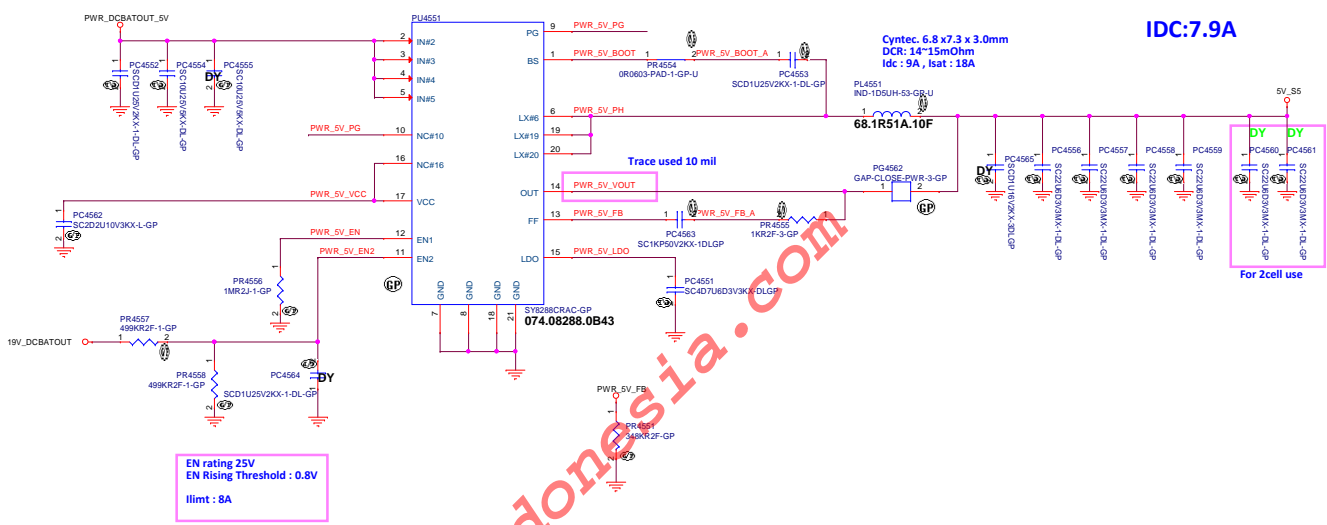
OFFPAGE-Signal



OFFPAGE-GAP

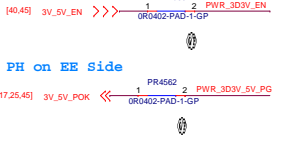


SY8288C For 5V

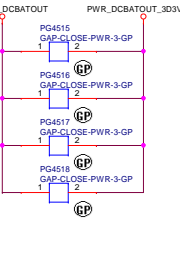


SSID = PWR.Plane.Regulator_3D3V

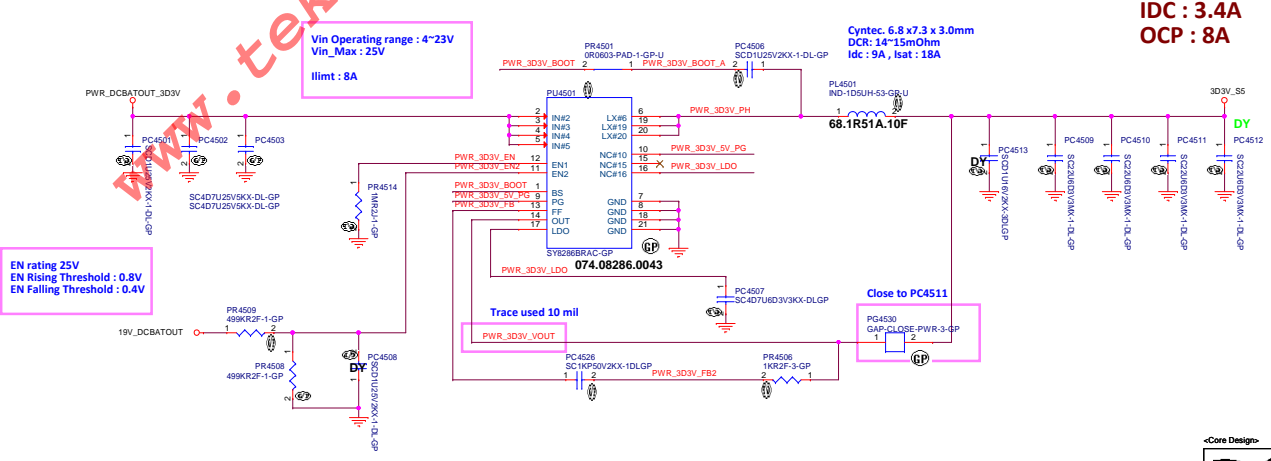
OFFPAGE-Signal



OFFPAGE-GAP



SY8286B For 3D3V



ISL95859C For CPUCORE

PH on CPU side

[3,24,44]	PROCHOT#_CPU	←←←
[7]	SVID_ALERT#_CPU	←←←
[7]	SVID_CLK_CPU	→→→
[7]	SVID_DATA_CPU	→→→
[44]	PWR_CORE_PSYS	→→→
[17,24,40]	VCCST_PWRIGD	→→→

For VCCGT Sense

同 VSSGT_SENSE

For Vcore Sense

```
[7] VDDCORE_SENSE >> _____
```

For Vccsa Sense

同	VSSA_SENSE	➡	
同	VCCA_SENSE	➡	

EE side Link

1V_VDDST_CPU

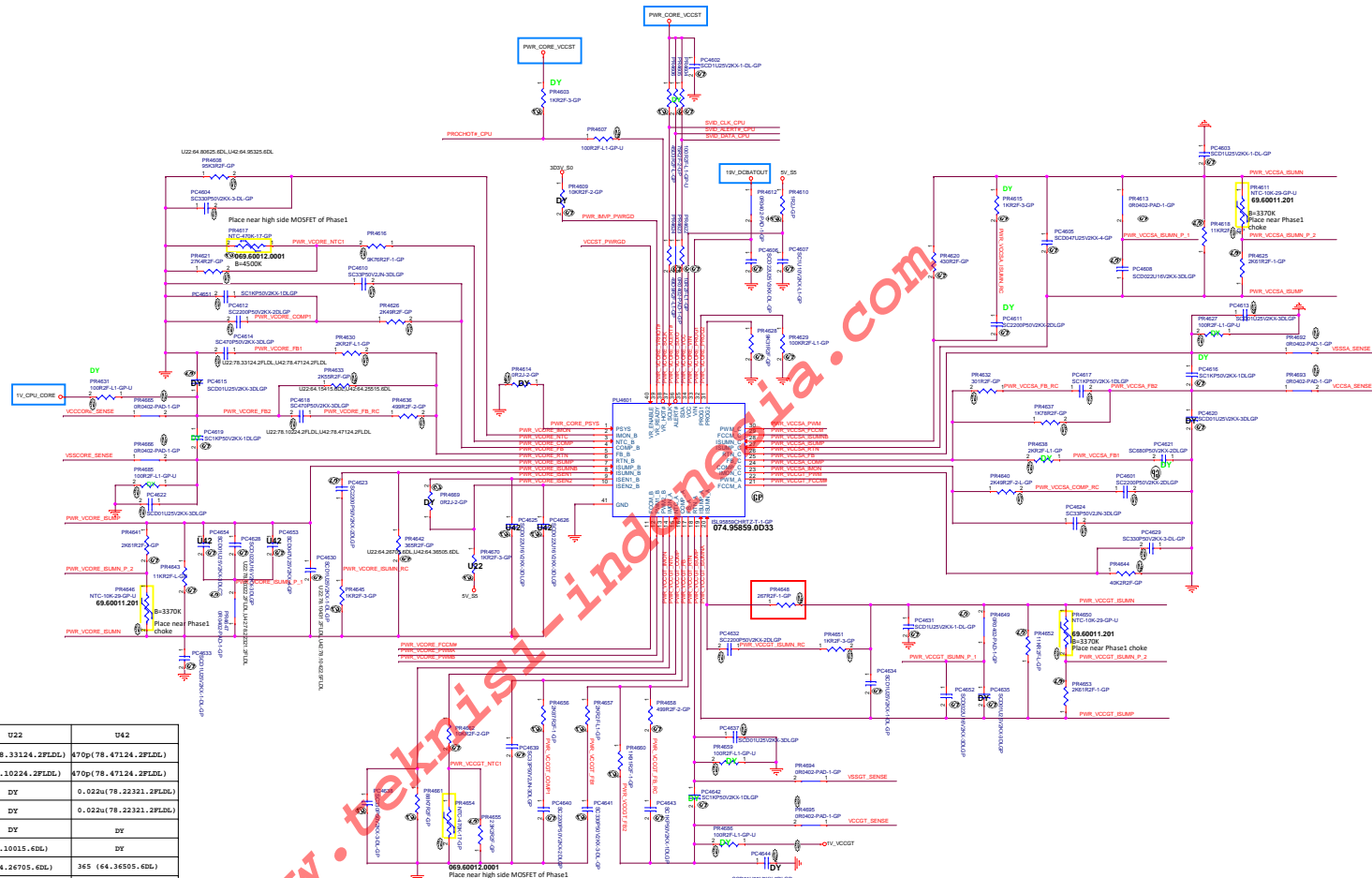
```

[47] PWR_VCORE_PVMB    >>>
[47] PWR_VCORE_S0UIN    >>>
[47] PWR_VCORE_S0UMP    >>>
[47] PWR_VCORE_F0COM    >>>
[47] PWR_VCORE_PVMA     >>>
[48] PWR_VCCGT_PVMB     >>>
[48] PWR_VCCGT_F0COM    >>>
[48] PWR_VCCGT_S0UIN    >>>
[48] PWR_VCCGT_S0UMP    >>>
[50] PWR_VCCSA_S0UMP    >>>
[50] PWR_VCCSA_S0UIN    >>>
[50] PWR_VCCSA_PVMB     >>>
[50] PWR_VCCSA_F0COM    >>>

```

[47] PWR_VCORE_ISEN1 >>>

[47] PWR_VCORE_ISEN2 >>>

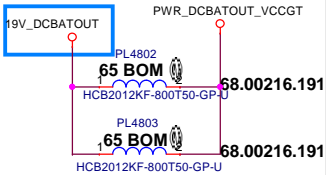


	U22	U42
PC4614	330P(78.13324,2PFLD)	470P(78.47124,2PFLD)
PC4618	1KP(78.10224,2PFLD)	470P(78.47124,2PFLD)
PC4625	DY	0.022u(78.22321,2PFLD)
PC4626	DY	0.022u(78.22321,2PFLD)
PR4669	DY	DY
PR4670	1K(64.15015,6DL)	345
PR4642	2u7(64.26705,6DL)	365 (64.26505,6DL)
PC4630	1.0uF(78.10431,2PFLD)	0.1uF(78.10422,5PFLD)
PC4628	0.01uF(78.10322,2PFLD)	22nF(78.20321,2PFLD)
PC4654	DY	0.01uF(78.12322,2PFLD)
PC4653	DY	47nF(078.47322,02FD)
PR4603	1.54K(64.15421,6DL)	2.55K(64.25521,6DL)
PR4608	80.6K(64.80625,6DL)	95.3K (64.95325,6DL)

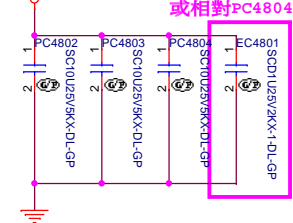
A00 20190530

Main Func = CPU_CORE

Offpage-Signal

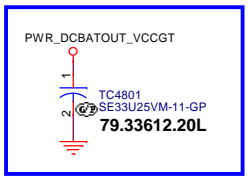


PWR_DCBATOUT_VCCGT



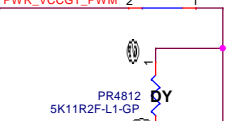
優先放在PC4804旁邊
或相對PC4804的Top層

For acoustic noise

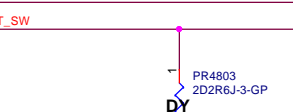
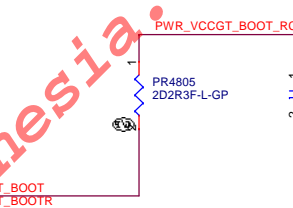
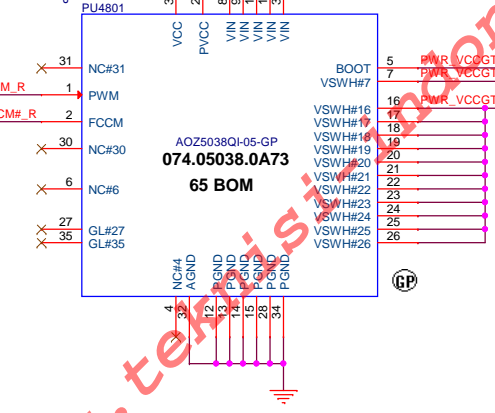
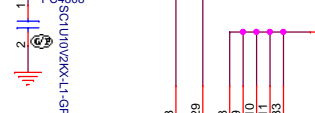
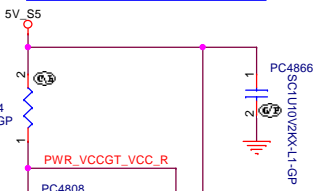


[46] PWR_VCCGT_PWM
[46] PWR_VCCGT_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN

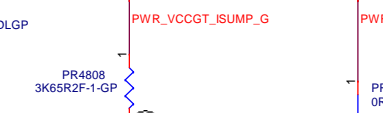
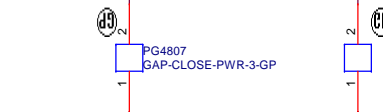
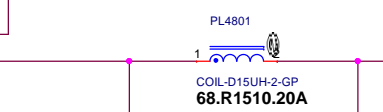
PR4802 0R0402-PAD-1-GP



PWR_VCCGT_FCCM#
PWR_VCCGT_FCCM#_R

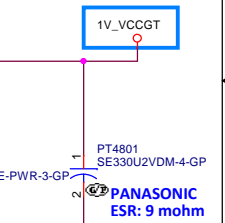


Cyntec 6.8mmx7.6mmx4.0mm
DCR: 0.66m ohm +/-7%
Idc : 36A , Isat : 45A



KBL_U22_15W
Icc(max)=31A
TDC=21A

Confirm with EE
22uF/0805 total 33pcs
(78.22610.L2L)



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RSVD

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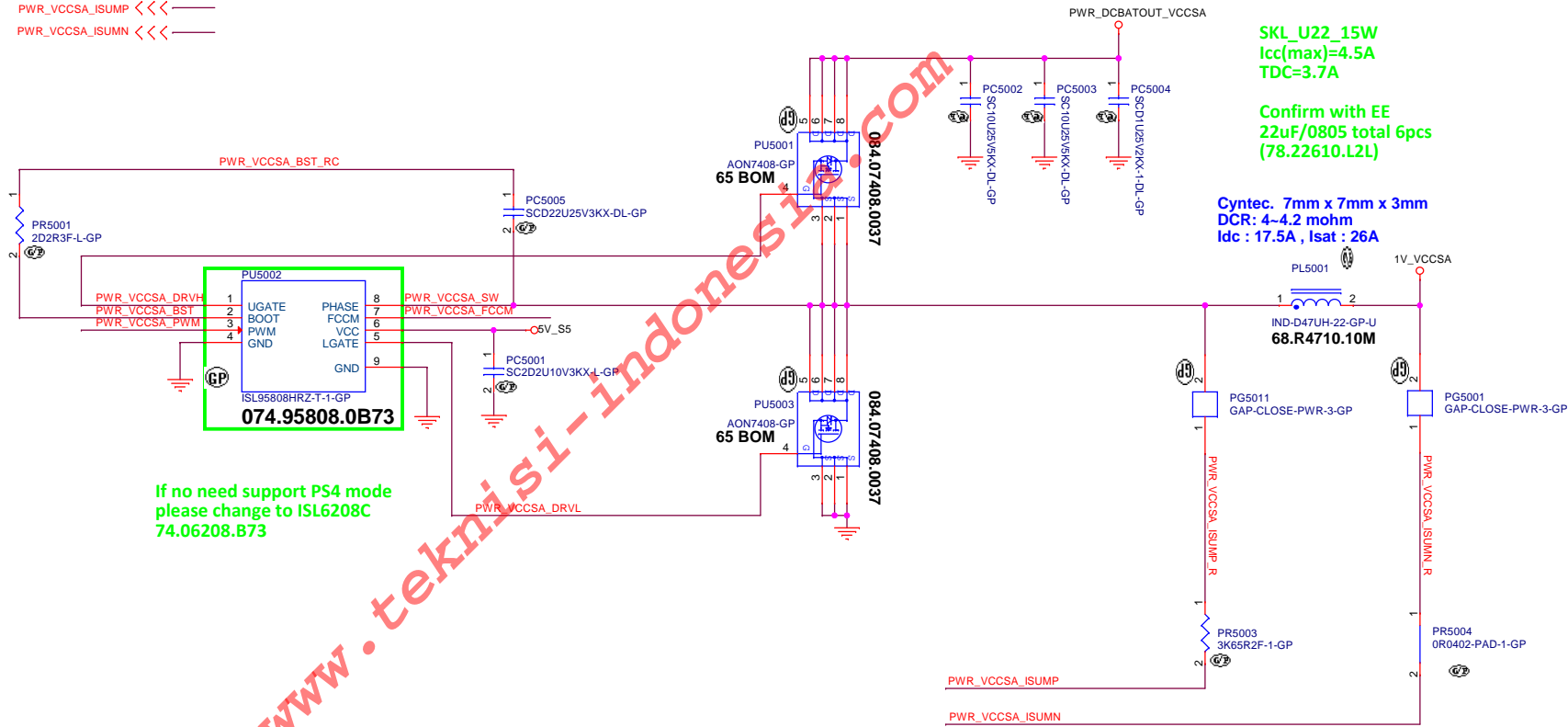
Title			POWER (CPU VCCGTS RSVD)	
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OFFPAGE



ISL95808 For VCCSA

- [46] PWR_VCCSA_PWM >>>
- [46] PWR_VCCSA_FCCM >>>
- [46] PWR_VCCSA_ISUMP <<<
- [46] PWR_VCCSA_ISUMN <<<



SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

Cyntec. 7mm x 7mm x 3mm
DCR: 4~4.2 mohm
Idc : 17.5A , Isat : 26A

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

SSID = PWR.Plane.Regulator_1D0V

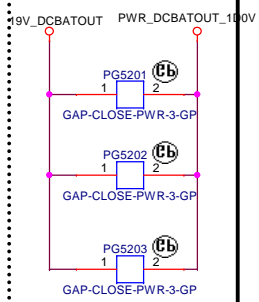
OFFPAGE-Signal

PH on EE Side

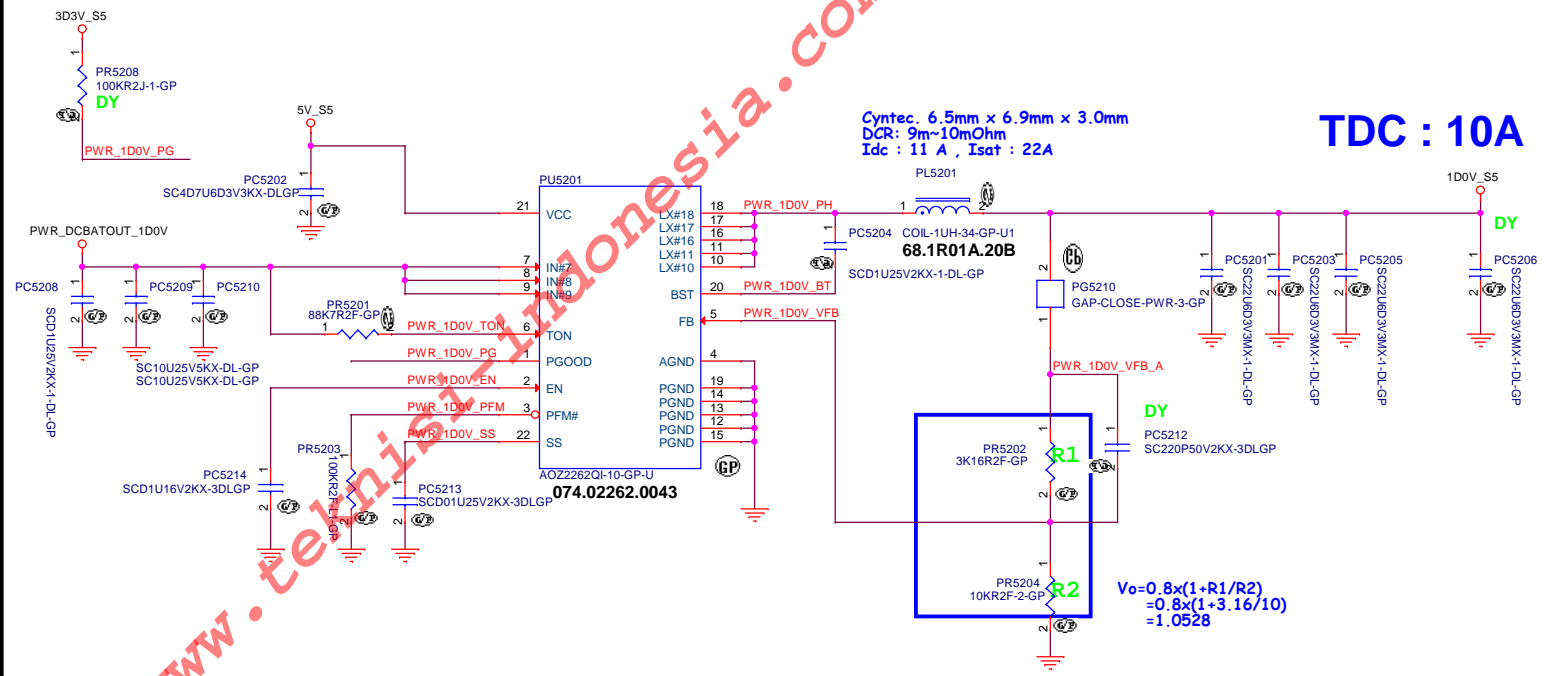
[40] 1D0V_S5_PWRGD << 1 PR5209 2 PWR_1D0V_PG
0R0402-PAD-1-GP

[25,53] 3V_5V_DSW_OK >> 2 PR5210 1 PWR_1D0V_EN
68KR2J-GP
fine tune power sequence

OFFPAGE-GAP

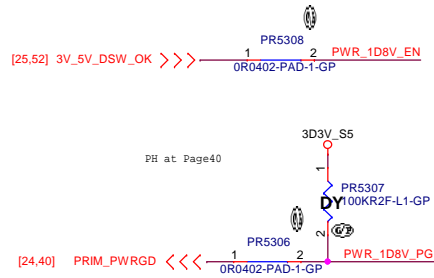


AOZ2262 For 1D05V

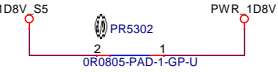


Main Func = 1D8V

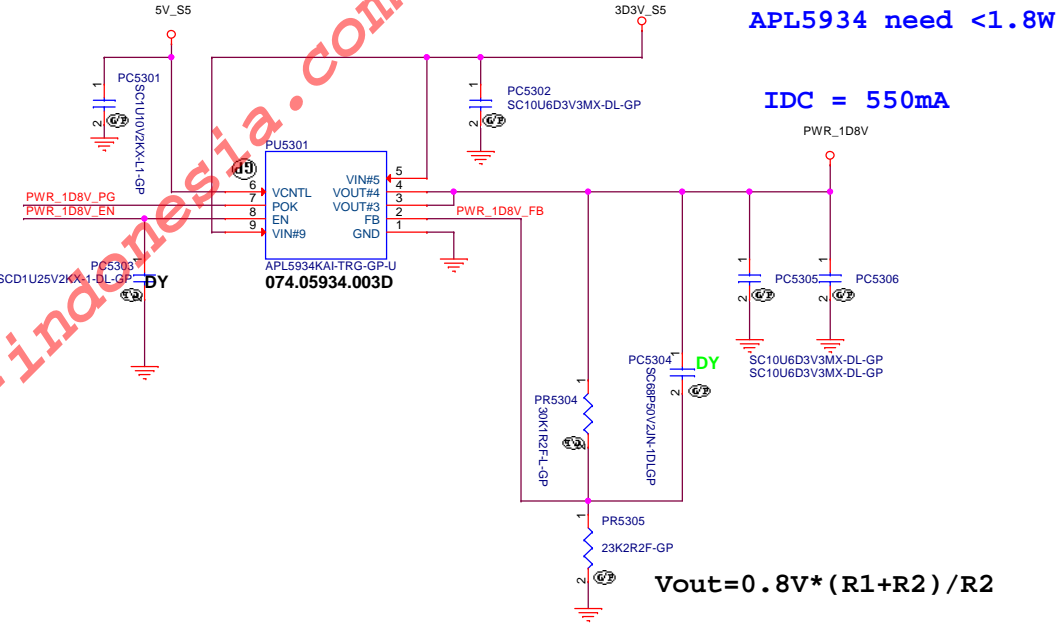
OFFPAGE



OFFPAGE_GAP




APL5934 for 1D8V



Main Func = 2D5V/ 1D8V

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Title

054 LDO-V1D8V&2D5V

Size

Document Number

Rev

A3

Mantis_CML

A00

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[0]	DBC_PANEL_EN	>>>	_____
[4]	EDP_VDD_EN	>>>	_____
[24]	LCD_VOC_TEST_EN	>>>	_____
[24]	LCD_TST	>>>	_____
[24]	BLON_OUT	>>>	_____
[4]	L_SKLT_CTRL	>>>	_____
[24]	TOUCH_REPORT_SW	>>>	_____
[64]	303W_LCDVDD_R	<<<	_____
[20]	CPU_GC_SCL_TS	<<<	_____
[20]	CPU_GC_SDA_TS	<<<	_____

PCB layout of the LCD driver IC 074.06288.00TB (2ND=074.00524.089F). The diagram shows the IC connected to a 3.3V supply, a 100k pull-up resistor, and an LCD panel. A note indicates the LCD panel is 100mm x 100mm. A detailed inset shows the connection of the LCD panel to the IC, with a note indicating the LCD panel is 100mm x 100mm.

0150-00

[16]	CCD_USB20_N	《》	_____
[16]	CCD_USB20_P	《》	_____
[16]	DMC_PCH_CLK	>>>	_____
[16]	DMC_PCH_DATA	>>>	_____
[27]	DMC_SCL_CODEC	>>>	_____
[27]	DMC_SDA_CODEC	>>>	_____

[illegible]

```

p1 TOUCH_PANEL_INTR# >>>_____
p1 TOUCH_PANEL_F0# >>>_____


```

[17,24]	PCH_RSMRSTW	⏏
[24,44,64]	HW_ACAV_IN	⏏
[24]	PANEL_MONITOR	⏏

Main Func = CRT

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Title

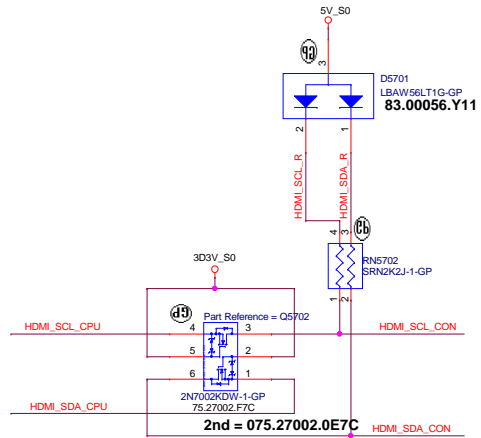
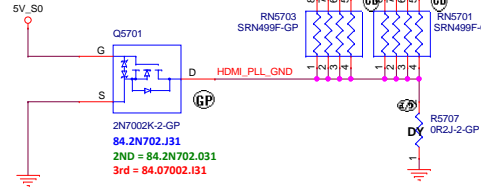
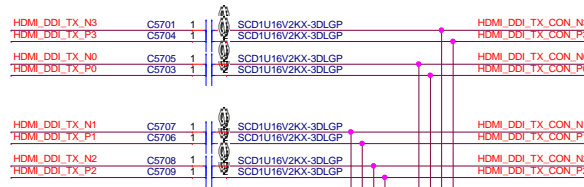
CRT(Reserved)

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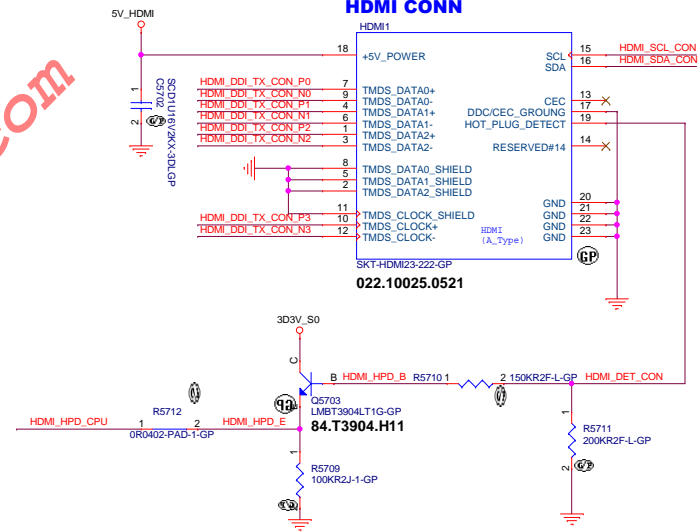
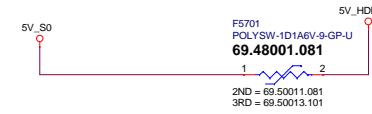
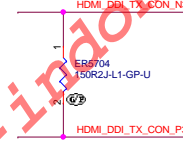
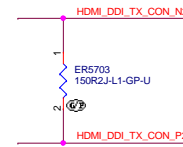
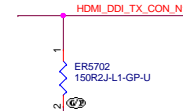
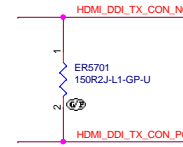
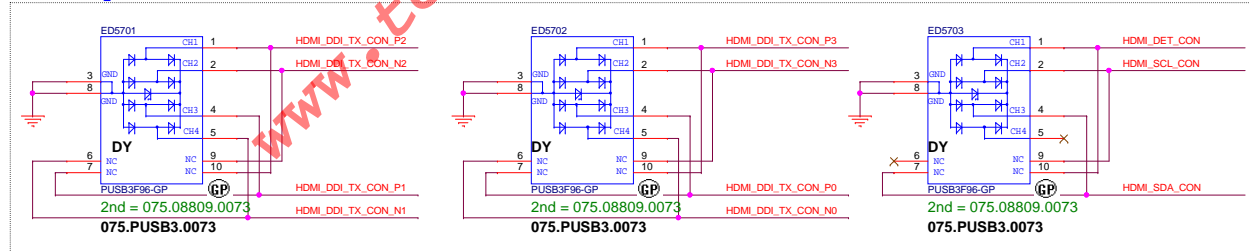
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SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0 >>>
 [4] HDMI_DDI_TX_P0 >>>
 [4] HDMI_DDI_TX_N1 >>>
 [4] HDMI_DDI_TX_P1 >>>
 [4] HDMI_DDI_TX_N2 >>>
 [4] HDMI_DDI_TX_P2 >>>
 [4] HDMI_DDI_TX_N3 >>>
 [4] HDMI_DDI_TX_P3 >>>
 [4] HDMI_SCL_CPU >>>
 [4] HDMI_SDA_CPU <<<
 [4] HDMI_HPD_CPU <<<



EMI Request:



<Core Design>

DELL		Wistron Corporation	
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Title		HDMI	
Size	Custom	Document Number	Mantis_CML
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Title			(Reserved)	
Size	Document Number	Rev		
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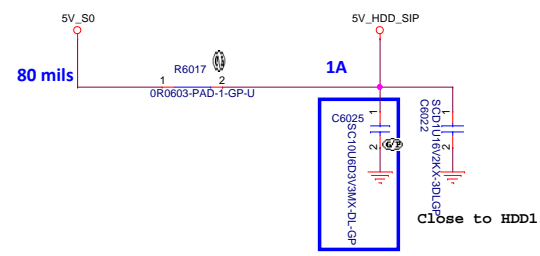
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			(Reserved)		
Size	Document Number				Rev
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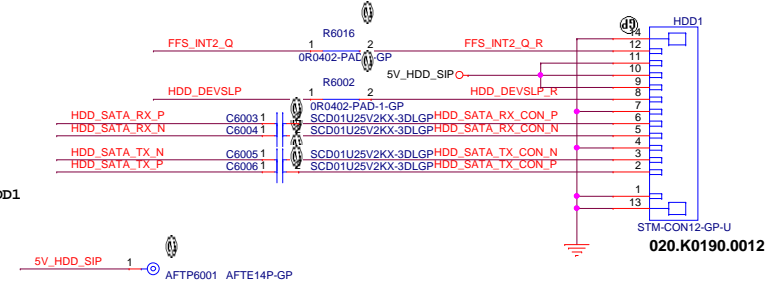
Main Func = HDD

HDD

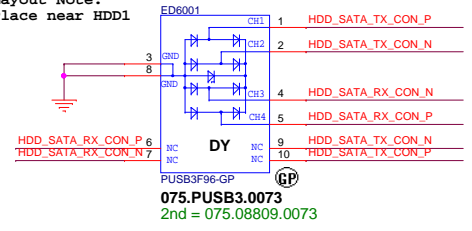
[16]	HDD_SATA_TX_P	>>>	
[16]	HDD_SATA_TX_N	>>>	
[16]	HDD_SATA_RX_P	<<<	
[16]	HDD_SATA_RX_N	<<<	
[70]	FFS_INT2_Q	>>	
[16]	HDD_DEVS_LP	>>	



SATA HDD Connector



Layout Note:
Place near HDD1



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Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N >>>—
[16] WLAN_PCIE_TX_P <<<—
[16] WLAN_PCIE_RX_N >>>—
[16] WLAN_PCIE_RX_P <<<—

PCIE_CLK

[18] WLAN_CLK_CPU_N >>>—
[18] WLAN_CLK_CPU_P <<<—
[18,61] WLAN_CLKREQ_CPU_N <<<—

USB2.0

[16] BT_USB20_P >>>—
[16] BT_USB20_N <<<—

Single end

[21] BLUETOOTH_EN >>>—
[21] WIFI_RF_EN >>>—
[17,63,66,76,91] PLT_RST# >>>—
[18,24] SUS_CLK >>>—

Power EN (Madesimo)

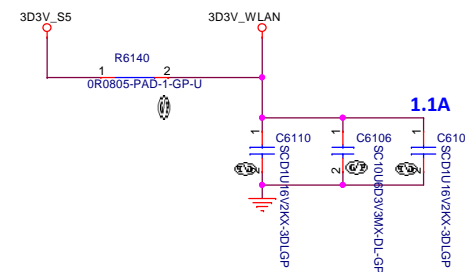
[19] BT_PCMOUT_CLKREQ0 >>>—
[19] BT_PCMFRM_CRF_RST_N >>>—

[21] CNV_WT_DN0 >>>—
[21] CNV_WT_DP0 >>>—
[21] CNV_WT_DN1 >>>—
[21] CNV_WT_DP1 >>>—
[21] CNV_WT_CLK_DN >>>—
[21] CNV_WT_CLK_DP >>>—

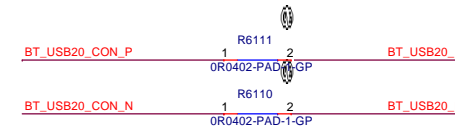
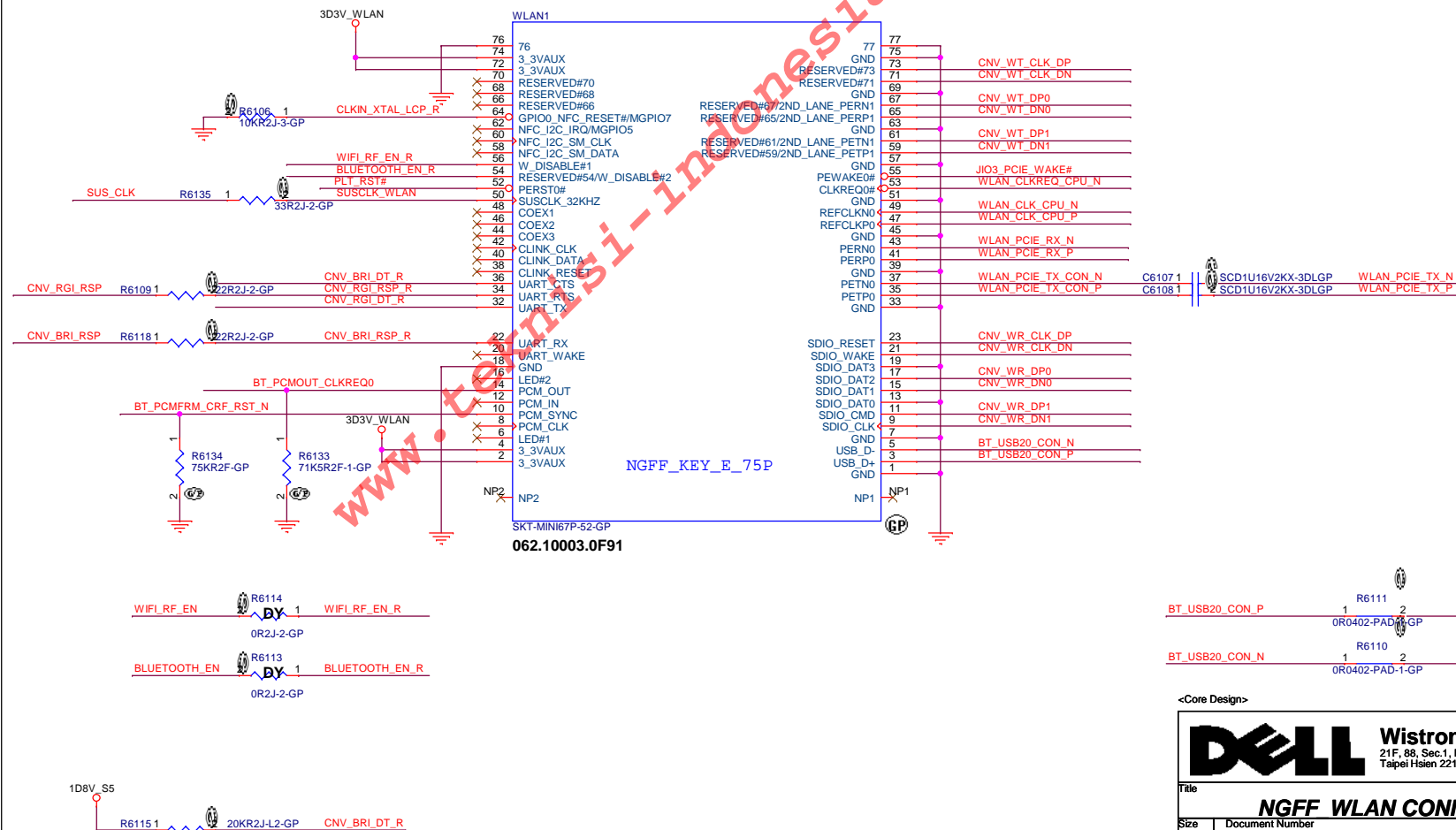
[21] CNV_WR_DN0 >>>—
[21] CNV_WR_DP0 >>>—
[21] CNV_WR_DN1 >>>—
[21] CNV_WR_DP1 >>>—
[21] CNV_WR_CLK_DN >>>—
[21] CNV_WR_CLK_DP >>>—

[15,20] CNV_RGI_DT_R >>>—
[20] CNV_BRI_DT_R >>>—
[20] CNV_BRI_RSP >>>—
[20] CNV_RGI_RSP >>>—

[18] JIO3_PCIE_WAKE# >>>—
[18] CLKN_XTAL_LCP_R >>>—



AFTE14P-GP	AFTP6101	1	3D3V_WLAN
AFTE14P-GP	AFTP6105	1	WLAN_CLKREQ_CPU_N
AFTE14P-GP	AFTP6106	1	WIFI_RF_EN_R
AFTE14P-GP	AFTP6107	1	BLUETOOTH_EN_R
AFTE14P-GP	AFTP6108	1	PLT_RST#
AFTE14P-GP	AFTP6109	1	BT_USB20_CON_N
AFTE14P-GP	AFTP6110	1	BT_USB20_CON_P
AFTE14P-GP	AFTP6608	1	JIO3_PCIE_WAKE#

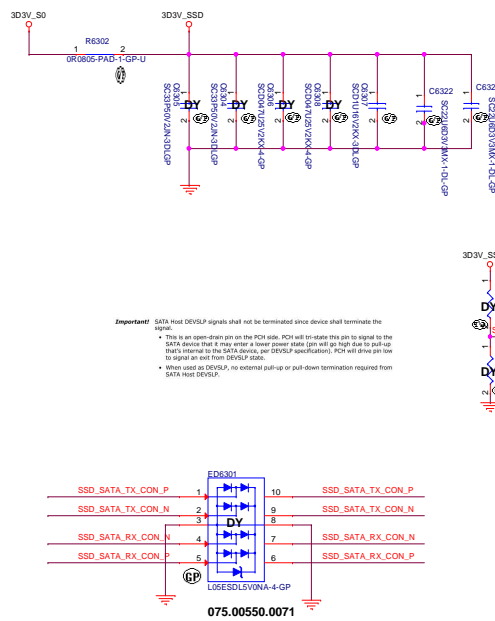
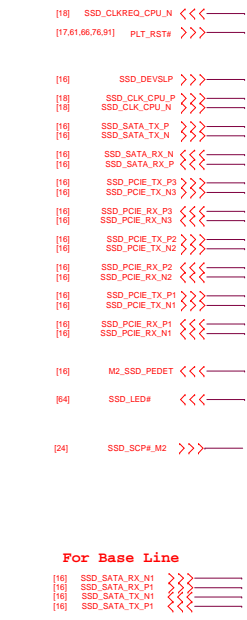


<Core Design>



Title			NGFF WLAN CONN		
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Main Func = M.2 SSD



SSD M.2 CONN

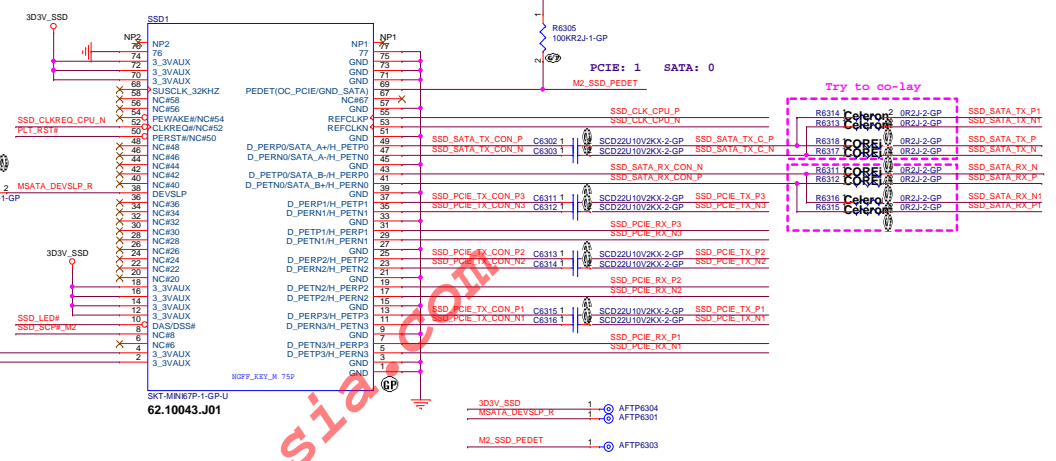


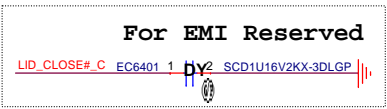
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal
1	SSD_SATA_TX_P1	19	SSD_SATA_TX_P1
2	SSD_SATA_TX_N1	20	SSD_SATA_TX_N1
3	SSD_SATA_RX_P1	21	SSD_SATA_RX_P1
4	SSD_SATA_RX_N1	22	SSD_SATA_RX_N1
5	SSD_SATA_TX_P2	23	SSD_SATA_TX_P2
6	SSD_SATA_TX_N2	24	SSD_SATA_TX_N2
7	SSD_SATA_RX_P2	25	SSD_SATA_RX_P2
8	SSD_SATA_RX_N2	26	SSD_SATA_RX_N2
9	SSD_SATA_TX_P3	27	SSD_SATA_TX_P3
10	SSD_SATA_TX_N3	28	SSD_SATA_TX_N3
11	SSD_SATA_RX_P3	29	SSD_SATA_RX_P3
12	SSD_SATA_RX_N3	30	SSD_SATA_RX_N3
13	SSD_SATA_TX_P4	31	SSD_SATA_TX_P4
14	SSD_SATA_TX_N4	32	SSD_SATA_TX_N4
15	SSD_SATA_RX_P4	33	SSD_SATA_RX_P4
16	SSD_SATA_RX_N4	34	SSD_SATA_RX_N4
17	SSD_SATA_TX_P5	35	SSD_SATA_TX_P5
18	SSD_SATA_TX_N5	36	SSD_SATA_TX_N5
19	SSD_SATA_RX_P5	37	SSD_SATA_RX_P5
20	SSD_SATA_RX_N5	38	SSD_SATA_RX_N5
21	SSD_SATA_TX_P6	39	SSD_SATA_TX_P6
22	SSD_SATA_TX_N6	40	SSD_SATA_TX_N6
23	SSD_SATA_RX_P6	41	SSD_SATA_RX_P6
24	SSD_SATA_RX_N6	42	SSD_SATA_RX_N6
25	SSD_SATA_TX_P7	43	SSD_SATA_TX_P7
26	SSD_SATA_TX_N7	44	SSD_SATA_TX_N7
27	SSD_SATA_RX_P7	45	SSD_SATA_RX_P7
28	SSD_SATA_RX_N7	46	SSD_SATA_RX_N7
29	SSD_SATA_TX_P8	47	SSD_SATA_TX_P8
30	SSD_SATA_TX_N8	48	SSD_SATA_TX_N8
31	SSD_SATA_RX_P8	49	SSD_SATA_RX_P8
32	SSD_SATA_RX_N8	50	SSD_SATA_RX_N8
33	SSD_SATA_TX_P9	51	SSD_SATA_TX_P9
34	SSD_SATA_TX_N9	52	SSD_SATA_TX_N9
35	SSD_SATA_RX_P9	53	SSD_SATA_RX_P9
36	SSD_SATA_RX_N9	54	SSD_SATA_RX_N9
37	SSD_SATA_TX_P10	55	SSD_SATA_TX_P10
38	SSD_SATA_TX_N10	56	SSD_SATA_TX_N10
39	SSD_SATA_RX_P10	57	SSD_SATA_RX_P10
40	SSD_SATA_RX_N10	58	SSD_SATA_RX_N10
41	SSD_SATA_TX_P11	59	SSD_SATA_TX_P11
42	SSD_SATA_TX_N11	60	SSD_SATA_TX_N11
43	SSD_SATA_RX_P11	61	SSD_SATA_RX_P11
44	SSD_SATA_RX_N11	62	SSD_SATA_RX_N11
45	SSD_SATA_TX_P12	63	SSD_SATA_TX_P12
46	SSD_SATA_TX_N12	64	SSD_SATA_TX_N12
47	SSD_SATA_RX_P12	65	SSD_SATA_RX_P12
48	SSD_SATA_RX_N12	66	SSD_SATA_RX_N12
49	SSD_SATA_TX_P13	67	SSD_SATA_TX_P13
50	SSD_SATA_TX_N13	68	SSD_SATA_TX_N13
51	SSD_SATA_RX_P13	69	SSD_SATA_RX_P13
52	SSD_SATA_RX_N13	70	SSD_SATA_RX_N13
53	SSD_SATA_TX_P14	71	SSD_SATA_TX_P14
54	SSD_SATA_TX_N14	72	SSD_SATA_TX_N14
55	SSD_SATA_RX_P14	73	SSD_SATA_RX_P14
56	SSD_SATA_RX_N14	74	SSD_SATA_RX_N14
57	SSD_SATA_TX_P15	75	SSD_SATA_TX_P15
58	SSD_SATA_TX_N15	76	SSD_SATA_TX_N15
59	SSD_SATA_RX_P15	77	SSD_SATA_RX_P15
60	SSD_SATA_RX_N15	78	SSD_SATA_RX_N15
61	SSD_SATA_TX_P16	79	SSD_SATA_TX_P16
62	SSD_SATA_TX_N16	80	SSD_SATA_TX_N16
63	SSD_SATA_RX_P16	81	SSD_SATA_RX_P16
64	SSD_SATA_RX_N16	82	SSD_SATA_RX_N16
65	SSD_SATA_TX_P17	83	SSD_SATA_TX_P17
66	SSD_SATA_TX_N17	84	SSD_SATA_TX_N17
67	SSD_SATA_RX_P17	85	SSD_SATA_RX_P17
68	SSD_SATA_RX_N17	86	SSD_SATA_RX_N17
69	SSD_SATA_TX_P18	87	SSD_SATA_TX_P18
70	SSD_SATA_TX_N18	88	SSD_SATA_TX_N18
71	SSD_SATA_RX_P18	89	SSD_SATA_RX_P18
72	SSD_SATA_RX_N18	90	SSD_SATA_RX_N18
73	SSD_SATA_TX_P19	91	SSD_SATA_TX_P19
74	SSD_SATA_TX_N19	92	SSD_SATA_TX_N19
75	SSD_SATA_RX_P19	93	SSD_SATA_RX_P19
76	SSD_SATA_RX_N19	94	SSD_SATA_RX_N19
77	SSD_SATA_TX_P20	95	SSD_SATA_TX_P20
78	SSD_SATA_TX_N20	96	SSD_SATA_TX_N20
79	SSD_SATA_RX_P20	97	SSD_SATA_RX_P20
80	SSD_SATA_RX_N20	98	SSD_SATA_RX_N20
81	SSD_SATA_TX_P21	99	SSD_SATA_TX_P21
82	SSD_SATA_TX_N21	100	SSD_SATA_TX_N21
83	SSD_SATA_RX_P21	101	SSD_SATA_RX_P21
84	SSD_SATA_RX_N21	102	SSD_SATA_RX_N21
85	SSD_SATA_TX_P22	103	SSD_SATA_TX_P22
86	SSD_SATA_TX_N22	104	SSD_SATA_TX_N22
87	SSD_SATA_RX_P22	105	SSD_SATA_RX_P22
88	SSD_SATA_RX_N22	106	SSD_SATA_RX_N22
89	SSD_SATA_TX_P23	107	SSD_SATA_TX_P23
90	SSD_SATA_TX_N23	108	SSD_SATA_TX_N23
91	SSD_SATA_RX_P23	109	SSD_SATA_RX_P23
92	SSD_SATA_RX_N23	110	SSD_SATA_RX_N23
93	SSD_SATA_TX_P24	111	SSD_SATA_TX_P24
94	SSD_SATA_TX_N24	112	SSD_SATA_TX_N24
95	SSD_SATA_RX_P24	113	SSD_SATA_RX_P24
96	SSD_SATA_RX_N24	114	SSD_SATA_RX_N24
97	SSD_SATA_TX_P25	115	SSD_SATA_TX_P25
98	SSD_SATA_TX_N25	116	SSD_SATA_TX_N25
99	SSD_SATA_RX_P25	117	SSD_SATA_RX_P25
100	SSD_SATA_RX_N25	118	SSD_SATA_RX_N25
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102	SSD_SATA_TX_N26	120	SSD_SATA_TX_N26
103	SSD_SATA_RX_P26	121	SSD_SATA_RX_P26
104	SSD_SATA_RX_N26	122	SSD_SATA_RX_N26
105	SSD_SATA_TX_P27	123	SSD_SATA_TX_P27
106	SSD_SATA_TX_N27	124	SSD_SATA_TX_N27
107	SSD_SATA_RX_P27	125	SSD_SATA_RX_P27
108	SSD_SATA_RX_N27	126	SSD_SATA_RX_N27
109	SSD_SATA_TX_P28	127	SSD_SATA_TX_P28
110	SSD_SATA_TX_N28	128	SSD_SATA_TX_N28
111	SSD_SATA_RX_P28	129	SSD_SATA_RX_P28
112	SSD_SATA_RX_N28	130	SSD_SATA_RX_N28
113	SSD_SATA_TX_P29	131	SSD_SATA_TX_P29
114	SSD_SATA_TX_N29	132	SSD_SATA_TX_N29
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121	SSD_SATA_TX_P31	139	SSD_SATA_TX_P31
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123	SSD_SATA_RX_P31	141	SSD_SATA_RX_P31
124	SSD_SATA_RX_N31	142	SSD_SATA_RX_N31
125	SSD_SATA_TX_P32	143	SSD_SATA_TX_P32
126	SSD_SATA_TX_N32	144	SSD_SATA_TX_N32
127	SSD_SATA_RX_P32	145	SSD_SATA_RX_P32
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134	SSD_SATA_TX_N34	152	SSD_SATA_TX_N34
135	SSD_SATA_RX_P34	153	SSD_SATA_RX_P34
136	SSD_SATA_RX_N34	154	SSD_SATA_RX_N34
137	SSD_SATA_TX_P35	155	SSD_SATA_TX_P35
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147	SSD_SATA_RX_P37	165	SSD_SATA_RX_P37
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149	SSD_SATA_TX_P38	167	SSD_SATA_TX_P38
150	SSD_SATA_TX_N38	168	SSD_SATA_TX_N38
151	SSD_SATA_RX_P38	169	SSD_SATA_RX_P38
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154	SSD_SATA_TX_N39	172	SSD_SATA_TX_N39
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157	SSD_SATA_TX_P40	175	SSD_SATA_TX_P40
158	SSD_SATA_TX_N40	176	SSD_SATA_TX_N40
159	SSD_SATA_RX_P40	177	SSD_SATA_RX_P40
160	SSD_SATA_RX_N40	178	SSD_SATA_RX_N40
161	SSD_SATA_TX_P41	179	SSD_SATA_TX_P41
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163	SSD_SATA_RX_P41	181	SSD_SATA_RX_P41
164	SSD_SATA_RX_N41	182	SSD_SATA_RX_N41
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167	SSD_SATA_RX_P42	185	SSD_SATA_RX_P42
168	SSD_SATA_RX_N42	186	SSD_SATA_RX_N42
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171	SSD_SATA_RX_P43	189	SSD_SATA_RX_P43
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231	SSD_SATA_RX_P58	249	SSD_SATA_RX_P58
232	SSD_SATA_RX_N58	250	SSD_SATA_RX_N58
233	SSD_SATA_TX_P59	251	SSD_SATA_TX_P59
234	SSD_SATA_TX_N59	252	SSD_SATA_TX_N59
235	SSD_SATA_RX_P59	253	SSD_SATA_RX_P59
236	SSD_SATA_RX_N59	254	SSD_SATA_RX_N59
237	SSD_SATA_TX_P60	255	SSD_SATA_TX_P60
238	SSD_SATA_TX_N60	256	SSD_SATA_TX_N60
239	SSD_SATA_RX_P60	257	SSD_SATA_RX_P60
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241	SSD_SATA_TX_P61	259	SSD_SATA_TX_P61
242	SSD_SATA_TX_N61	260	SSD_SATA_TX_N61
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244	SSD_SATA_RX_N61	262	SSD_SATA_RX_N61
245	SSD_SATA_TX_P62	263	SSD_SATA_TX_P62
246	SSD_SATA_TX_N62	264	SSD_SATA_TX_N62
247	SSD_SATA_RX_P62	265	SSD_SATA_RX_P62
248	SSD_SATA_RX_N62	266	SSD_SATA_RX_N62
249	SSD_SATA_TX_P63	267	SSD_SATA_TX_P63
250	SSD_SATA_TX_N63	268	SSD_SATA_TX_N63
251	SSD_SATA_RX_P63	269	SSD_SATA

Main Func = Power BTN

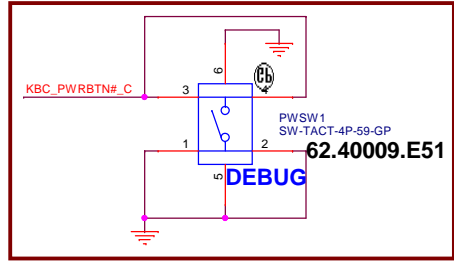
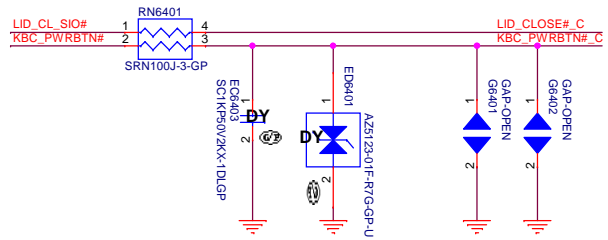
[20,24] LID_CL_SIO# <<< _____
[24] KBC_PWRBTN# <<< _____
[67,92] LID_CLOSE#_C >>> _____

Low activated from KBC GPIO



Power button

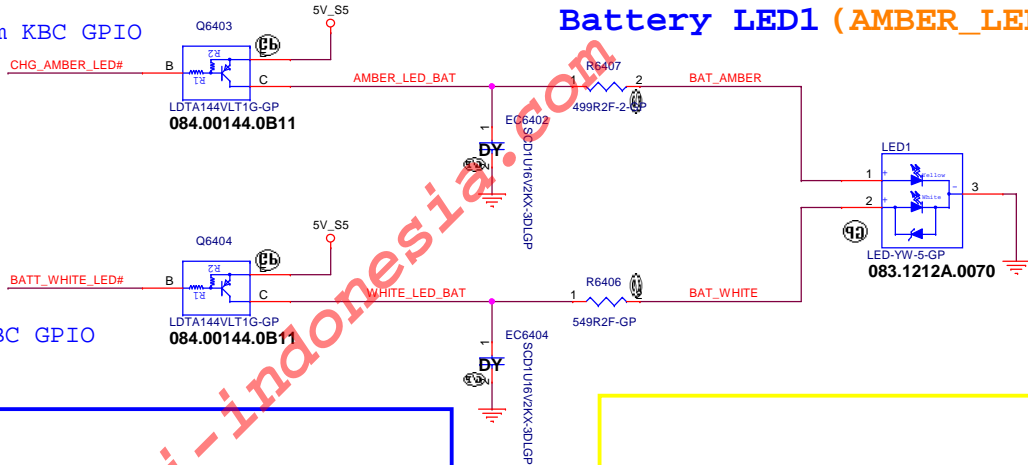
Layout note:
G6401 place to bottom
G6402 place to top



[92] KBC_PWRBTN#_C <<< _____
[17] PM_RSMRST# >>> _____
[24,44] HW_ACAV_IN >>> _____

Low activated from KBC GPIO

Battery LED1 (AMBER_LED)

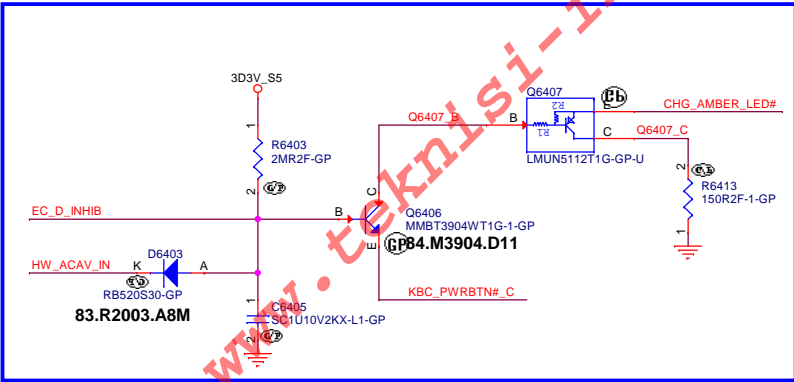


Main Func = Battery LED

[24] CHG_AMBER_LED# >>> _____
[24] EC_D_INHIB <<< _____
[24] BATT_WHITE_LED# >>> _____

Low activated from KBC GPIO

M-BIST

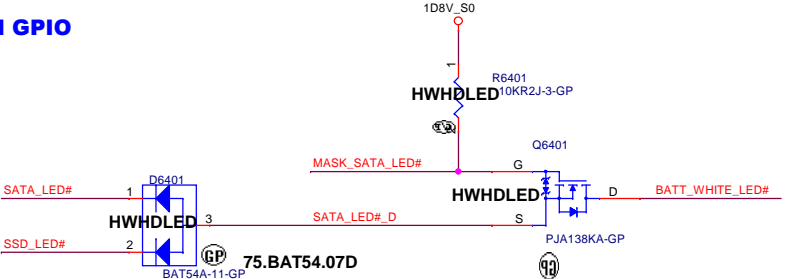


Battery LED2 (WHITE_LED)

Main Func = HDD LED

[24] MASK_SATA_LED# >>> _____
[16] SATA_LED# >>> _____
[63] SSD_LED# >>> _____

SATA HDD LED
LOW activated from PCH GPIO



<Core Design>

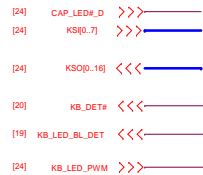
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: **LED Board&Power Button**

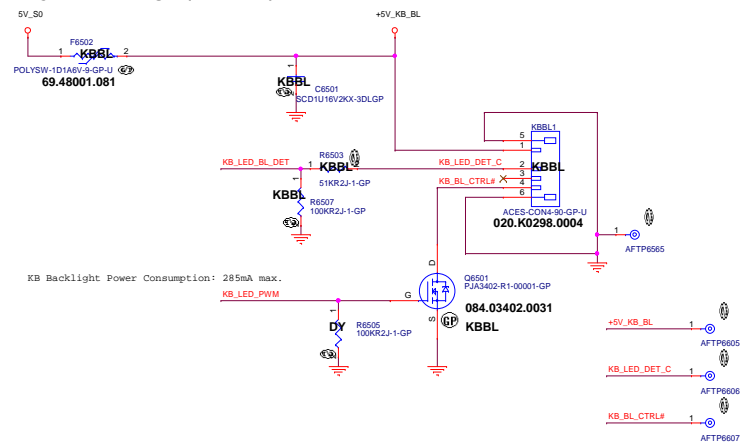
Size A3 Document Number: **Mantis CML** Rev: **A00**

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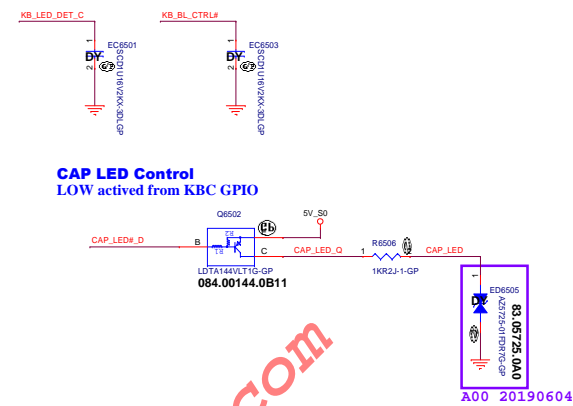
Main Func = KB



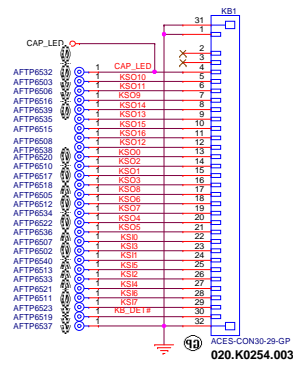
Keyboard Backlight (Reserved)



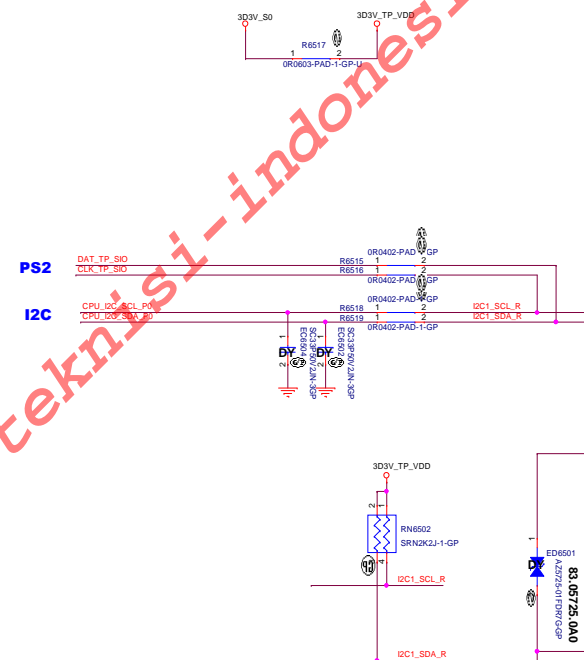
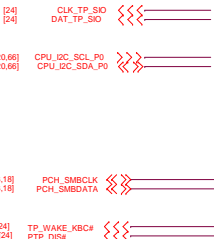
CAP LED Control
LOW actived from KBC GPIO



Internal Keyboard Connector

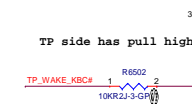


Main Func = TPAD

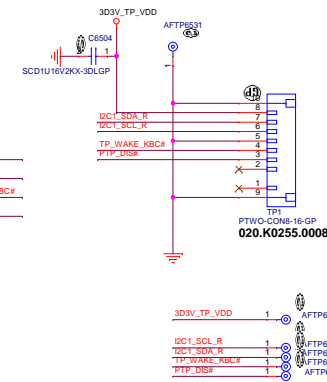


Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

TP side has pull high



Precision Touch Pad Connector



USB2.0

```
[16] USB3_USB20_N  << >> _____
[16] USB3_USB20_P  << >> _____
```

Card Reder

[16] CARD1_USB20_N << >> _____

[16] CARD1_USB20_P << >> _____

LAN

[16]	LAN_PCIE_RX_N	>>>>	_____
[16]	LAN_PCIE_RX_P	>>>>	_____
[16]	LAN_PCIE_TX_N	>>>>	_____
[16]	LAN_PCIE_TX_P	>>>>	_____
[18]	LAN_CLK_CPU_N	>>>>	_____
[18]	LAN_CLK_CPU_P	>>>>	_____
[18]	LAN_CLKREQ_CPU_N	>>>>	_____
[24]	PM_LAN_ENABLE	>>>>	_____
[24]	LANWAKE#_IC	>>>>	_____

To audio jack on DB.

[27,29]	AUD_RING	<<<	_____
[27,29]	AUD_SLEEVE	<<<	_____
[29]	AUD_HP1_JACK_L1	<<<	_____
[29]	AUD_HP1_JACK_R1	<<<	_____
[27]	AUD_SENSE	>>>	_____

[17,61,63,76,91] PLT_RST# >>>_____

[55] 3D3V_LCDVDD_R >>> _____

[20,65] CPU_I2C_SCL_P0 <<< _____

[20,65] CPU_I2C_SDA_P0 <<< _____

```
[44] PWR_CHG_CSOP_R  >>> _____
[44] PWR_CHG_CSON_R  >>> _____
```

Pin define by follow layout routing

I/O Board Connector

Pitch: 0.5mm

Power: 6 pins

GND: 4 pins

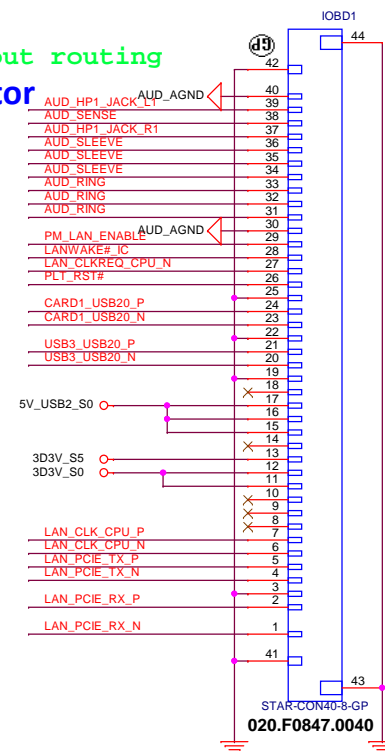
Wire

Card Reader

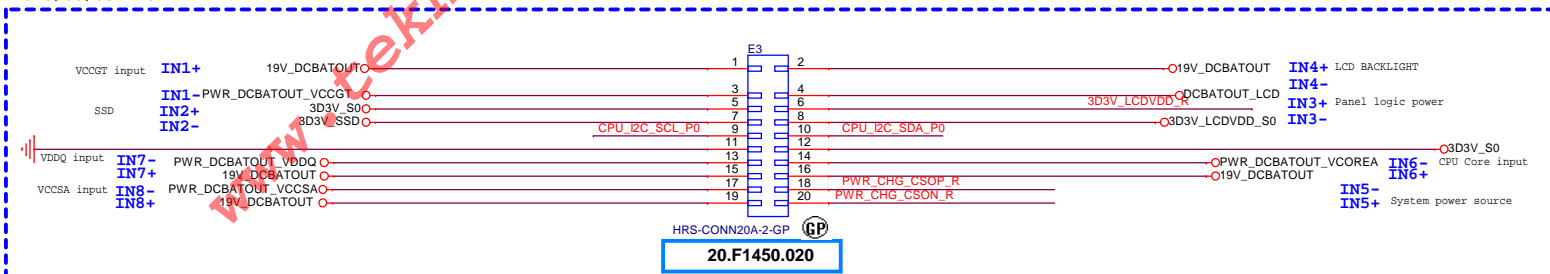
USB2.0 port 3

FP /Card Reder power

Coaxial



2018/05/03 E3



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Title

IO Board Connector

Size

Document Number	
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Rev

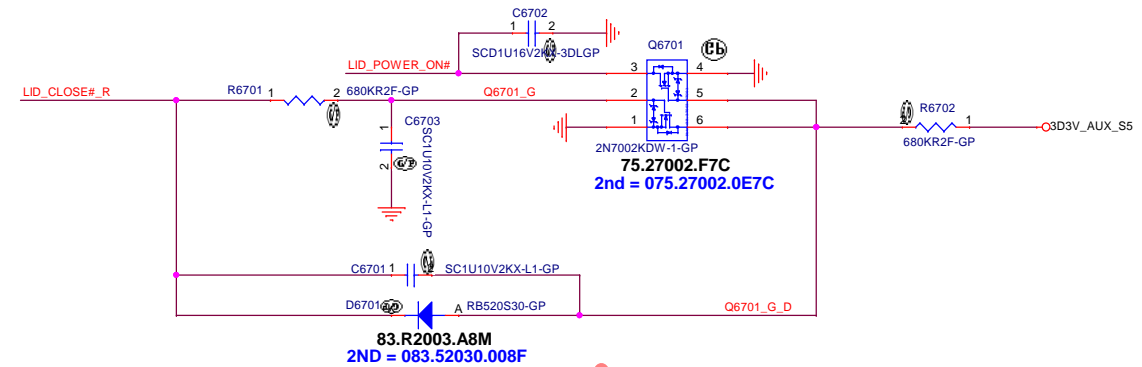
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```
Main Func = HALL SENSOR
```

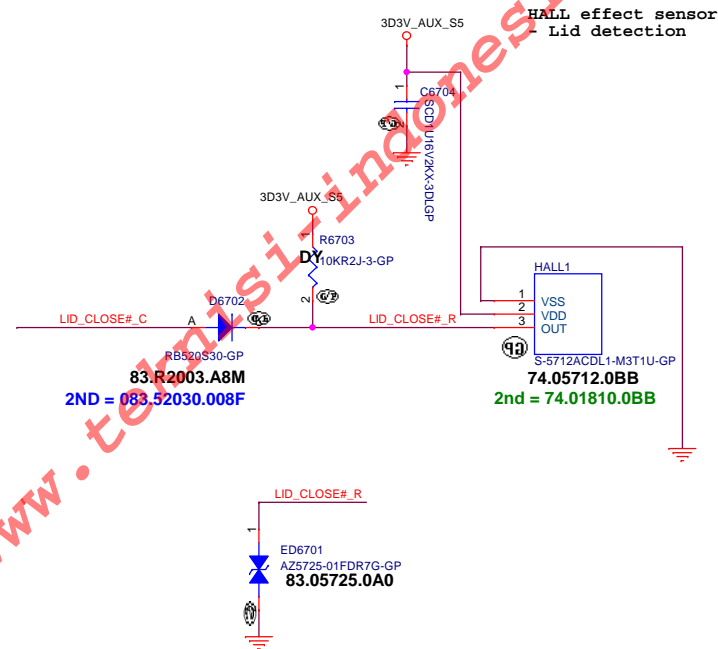
LID sensor



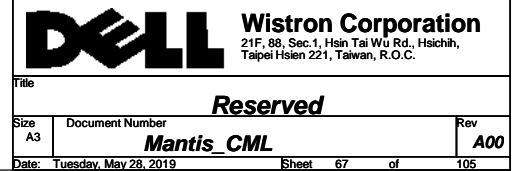
[24] LID_POWER_ON# >>> _____

[64,92] LID_CLOSE#_C <<<_____

LID sensor



<Core Design>

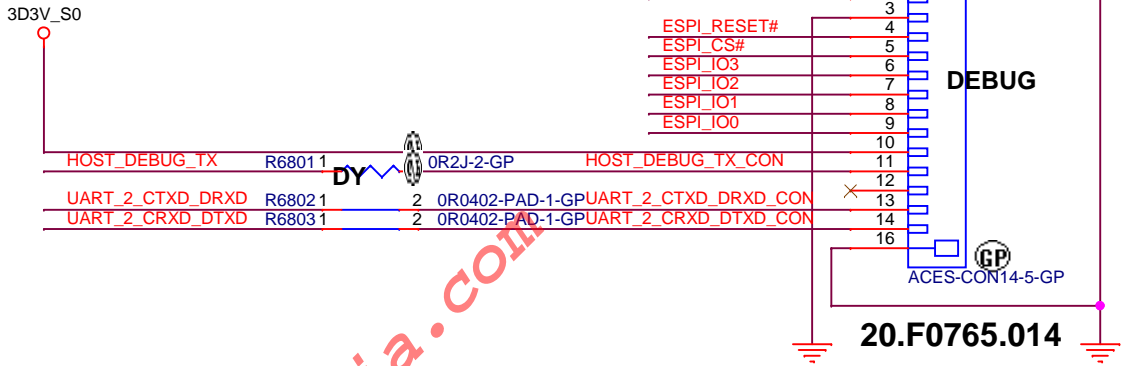
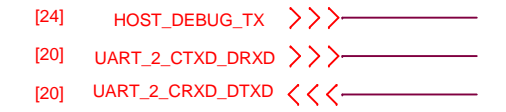


Main Func = Debug

ESPI



UART



ESPI Debug Connector

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Title Dubug connector			
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A4

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Title

RESERVED

Size
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Rev
A00

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Main Func =TI

[74] PD_VBUS_C_CTRL1 <<<

EC

[24] TYPEC_SMBDA >>>

[24] TYPEC_SMBCLK >>>

[74] VBUS_P_CTRL <<<

MUX TUSB546

[73] I2C_DATA_PD >>>

[73] I2C_CLK_PD >>>

[4,73] DP1_HPD_CPU <<<

[24,72] UPD1_SMBINT# <<<

[73] CCG5_SBU1 <<<

[73] CCG5_SBU2 <<<

[74] NXP3290_F0 >>>

[24,72] UPD1_SMBINT# <<<

TYPE-C CONNECTOR

[73] USB1_CC1 >>>

[73] USB1_CC2 >>>

[73] TOP_MUX_P_L >>>

[73] TOP_MUX_N_L >>>

[73] BOT_MUX_P_L >>>

[73] BOT_MUX_N_L >>>

[73] USB1_SBU1 <<<

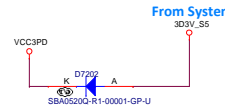
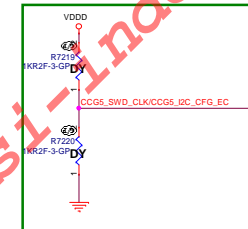
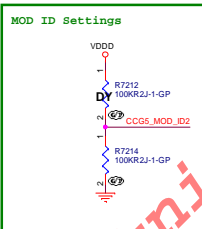
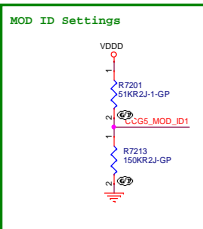
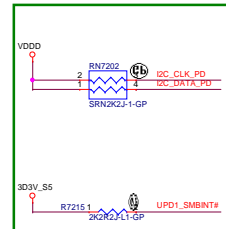
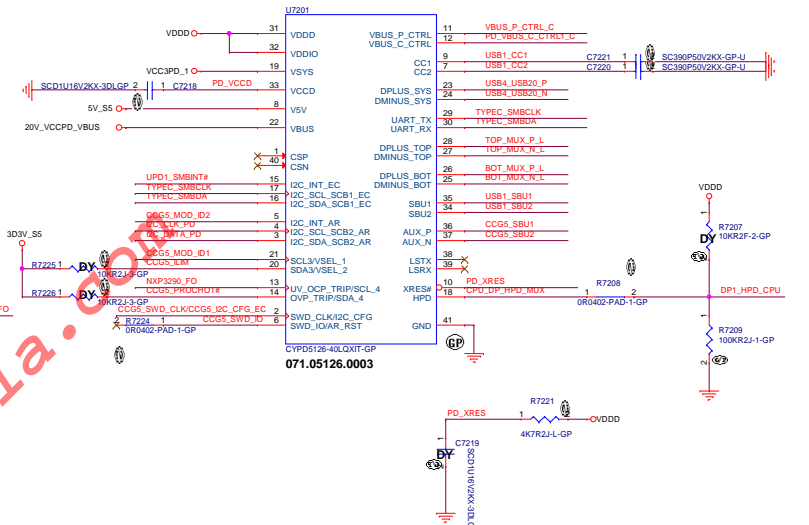
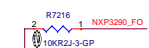
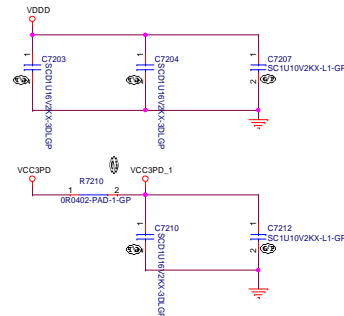
[73] USB1_SBU2 <<<

PCH

[16] USB4_USB20_P >>>

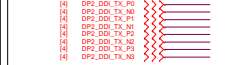
[16] USB4_USB20_N >>>

Power

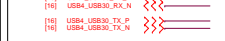


Main Func = TYPEC MUX

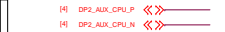
DisplayPort Source



USB HOST



DisplayPort AUX



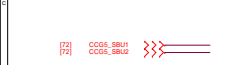
MUX I2C



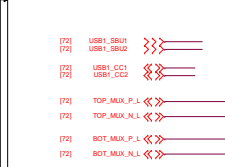
DisplayPort HPD



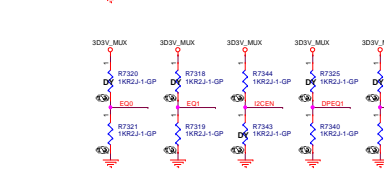
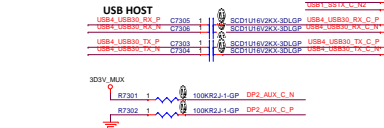
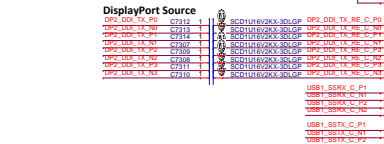
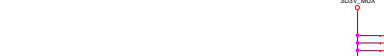
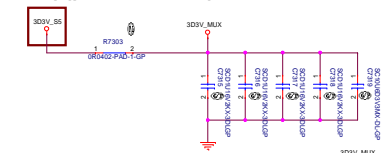
I2C/USB MUX



TypeC CC

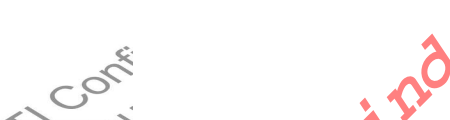
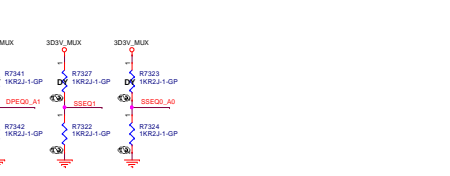
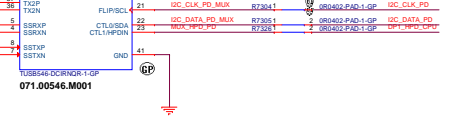
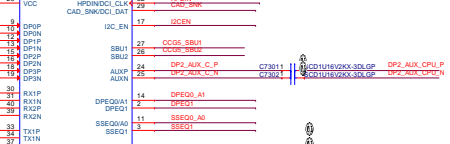
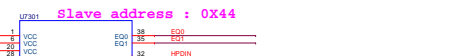


For displayport function at dead battery condition

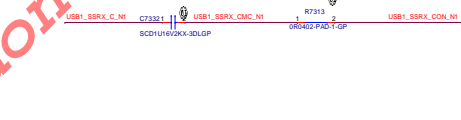
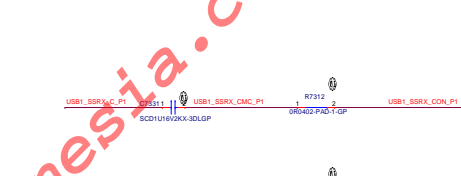
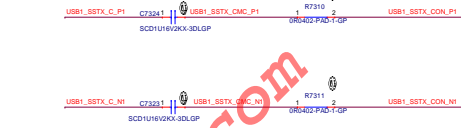


CODE	NAME	INIT	Mux Operation
X	LOW	LOW	POWER_DOWN
LOW	LOW	W100H	4-Lane Orientation 1
LOW	W100H	W100H	4-Lane Orientation 2
LOW	W100H	W100H	2-Lane Orientation 1
LOW	W100H	W100H	2-Lane Orientation 2
LOW	W100H	LOW	USB3.1 only Orientation 1
LOW	W100H	LOW	USB3.1 only Orientation 2

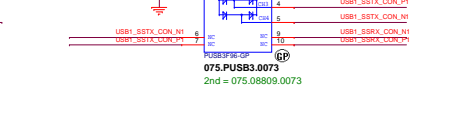
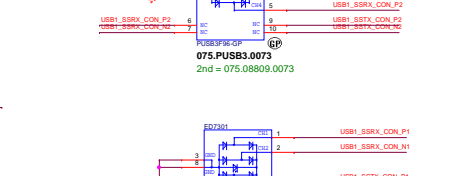
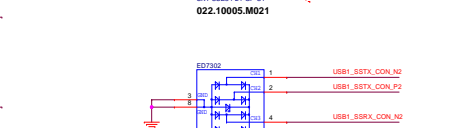
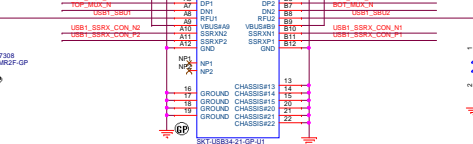
CODE	NAME	INIT	Mux Operation
2-3	W100H/W100H	W100H	4-Lane Orientation 1
2-3	W100H/W100H	W100H	4-Lane Orientation 2
2-3	W100H/W100H	W100H	2-Lane Orientation 1
2-3	W100H/W100H	W100H	2-Lane Orientation 2
2-3	W100H/W100H	W100H	USB3.1 only Orientation 1
2-3	W100H/W100H	W100H	USB3.1 only Orientation 2



CODE	NAME	INIT	Mux Operation
X	LOW	LOW	POWER_DOWN
LOW	LOW	W100H	4-Lane Orientation 1
LOW	W100H	W100H	4-Lane Orientation 2
LOW	W100H	W100H	2-Lane Orientation 1
LOW	W100H	W100H	2-Lane Orientation 2
LOW	W100H	LOW	USB3.1 only Orientation 1
LOW	W100H	LOW	USB3.1 only Orientation 2



CODE	NAME	INIT	Mux Operation
X	LOW	LOW	POWER_DOWN
LOW	LOW	W100H	4-Lane Orientation 1
LOW	W100H	W100H	4-Lane Orientation 2
LOW	W100H	W100H	2-Lane Orientation 1
LOW	W100H	W100H	2-Lane Orientation 2
LOW	W100H	LOW	USB3.1 only Orientation 1
LOW	W100H	LOW	USB3.1 only Orientation 2



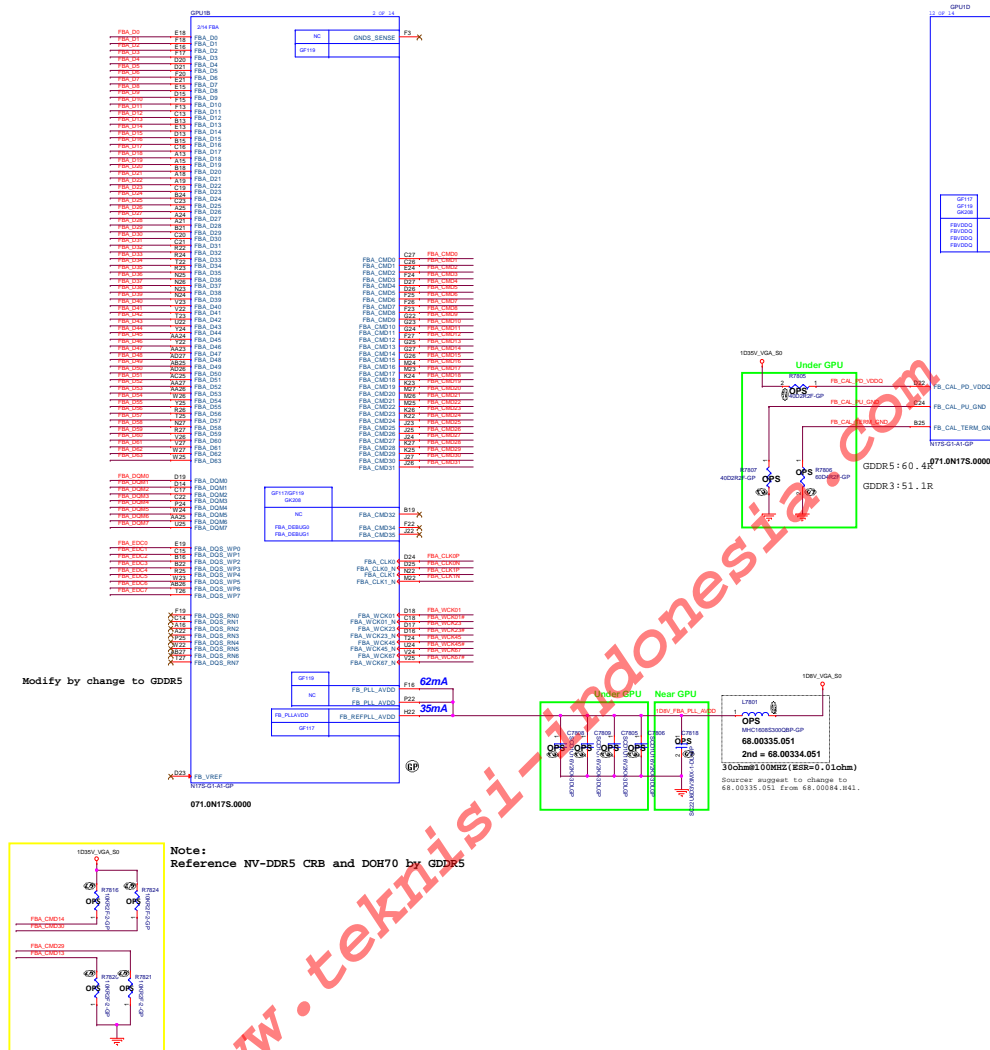
CODE	NAME	INIT	Mux Operation
X	LOW	LOW	POWER_DOWN
LOW	LOW	W100H	4-Lane Orientation 1
LOW	W100H	W100H	4-Lane Orientation 2
LOW	W100H	W100H	2-Lane Orientation 1
LOW	W100H	W100H	2-Lane Orientation 2
LOW	W100H	LOW	USB3.1 only Orientation 1
LOW	W100H	LOW	USB3.1 only Orientation 2

[illegible]

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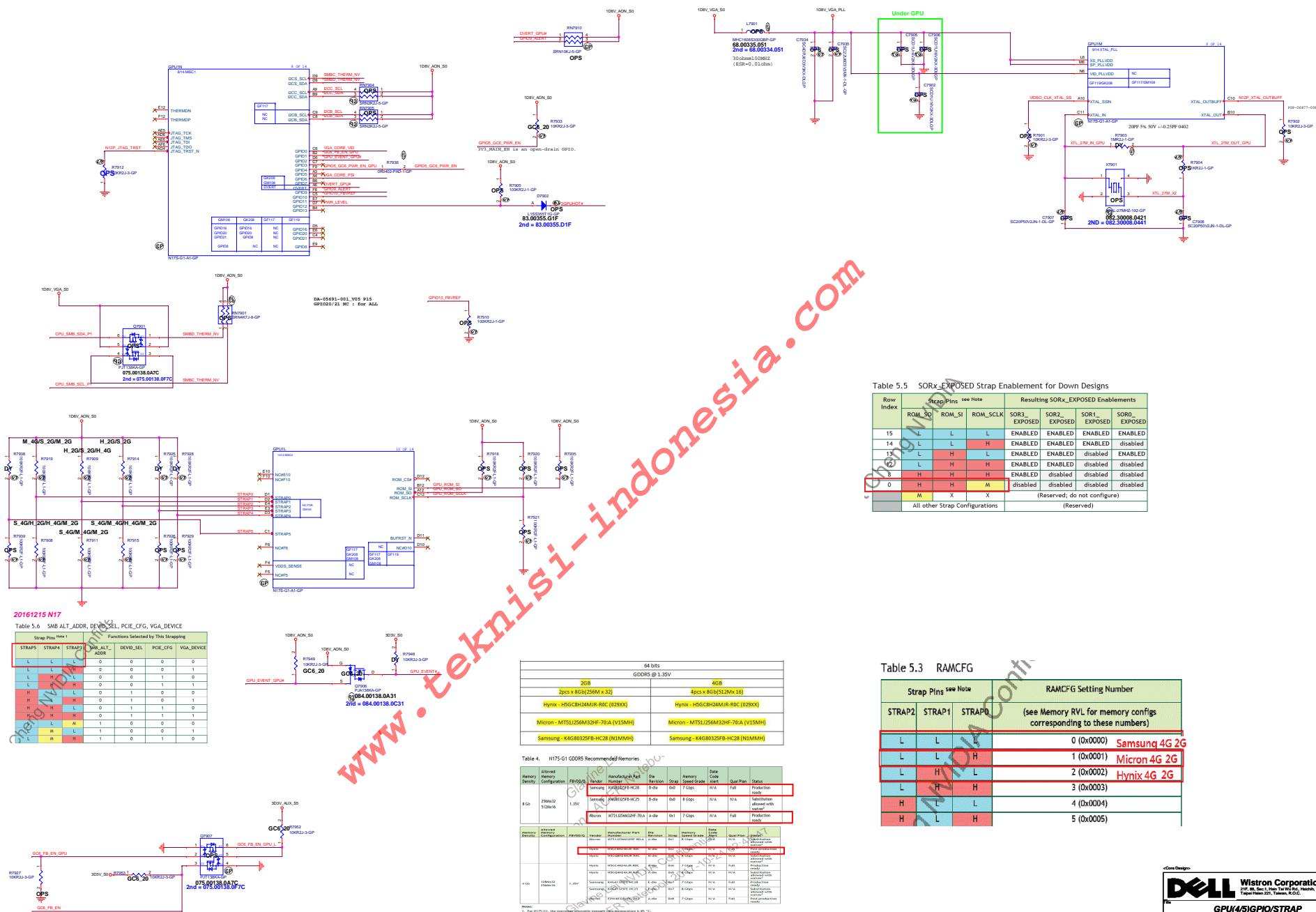
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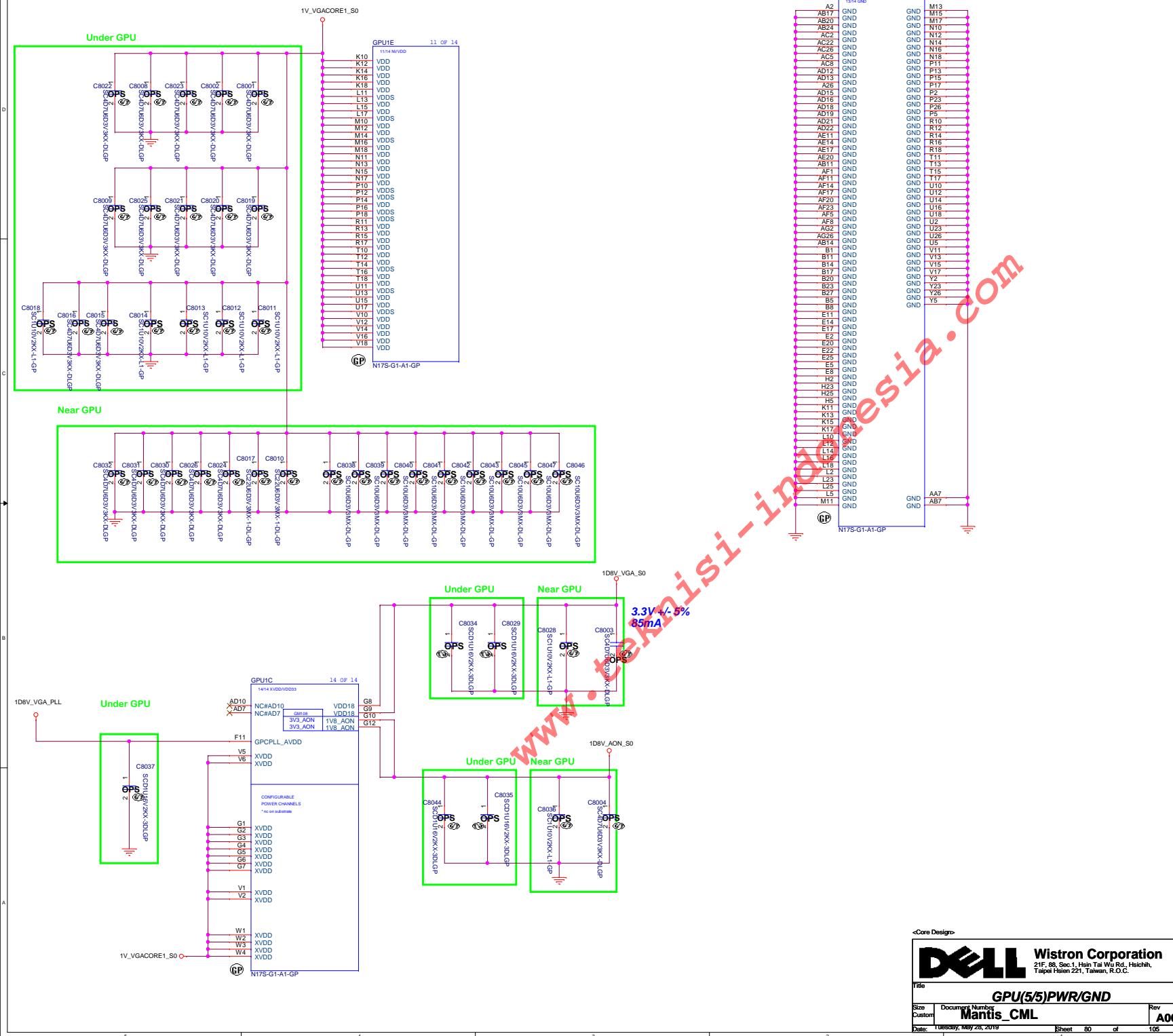
[illegible]

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/Q Supply Rail for GDDR5						
GB28-64, GB2C-64	0.1 μ F	X7R	0402	2	0	Under GPU
	1 μ F	X7R	0603	2	8	Under GPU
	4.7 μ F	X6S	0603	2	0	Under GPU
	10 μ F	X6S	0603	0	2	Under GPU
	10 μ F	X6S	0603	1	1	Near GPU
	22 μ F	X6S	0603W	1	3	Near GPU

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FB PLL Supply Rail for GDR05						
GB2B-64, GB2C-64	0.1 μ F	X7R	0402	2	4	Under GPU
	22 μ F	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)	0603	1	1	1	Near GPU

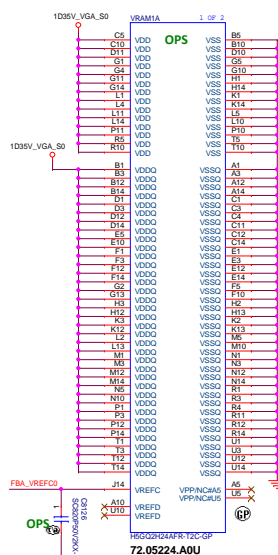
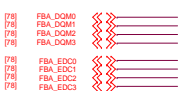
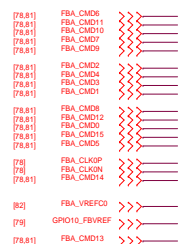


Main Func = dGPU

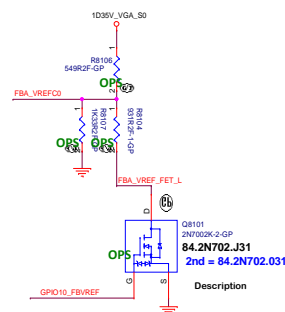


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Title			
GPU(5/5)PWR/GND			
Size	Document Number	Rev	
Custom	Mantis_CML	A00	
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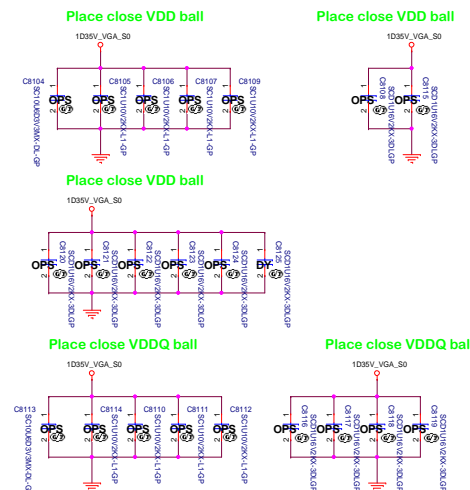
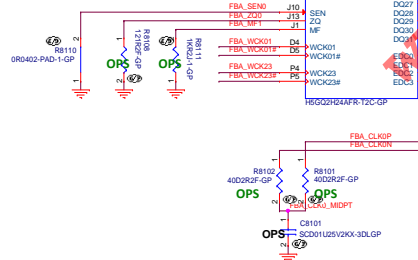
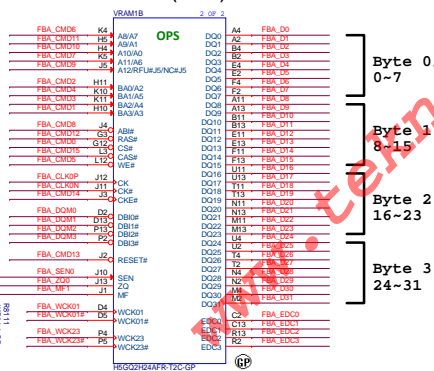
Frame Buffer Partition A-Lower Half



FBVREF Termination

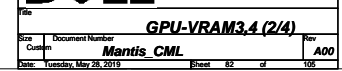
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Normal(MF=0)




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Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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GPU-VRAM5,6 (3/4)

Size

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Document Number

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Title

GPU-VRAM7,8 (4/4)

Size
A3

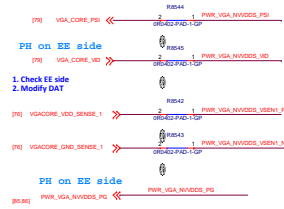
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OFFPAGE-GAP



EE need check

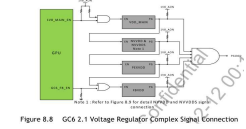
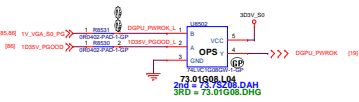
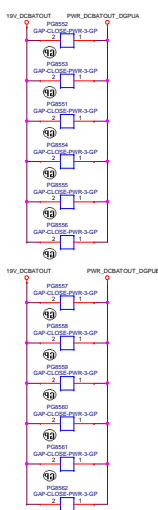
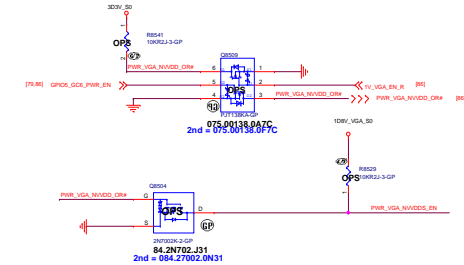


Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection



For VGA_CORE sequence
EE need check

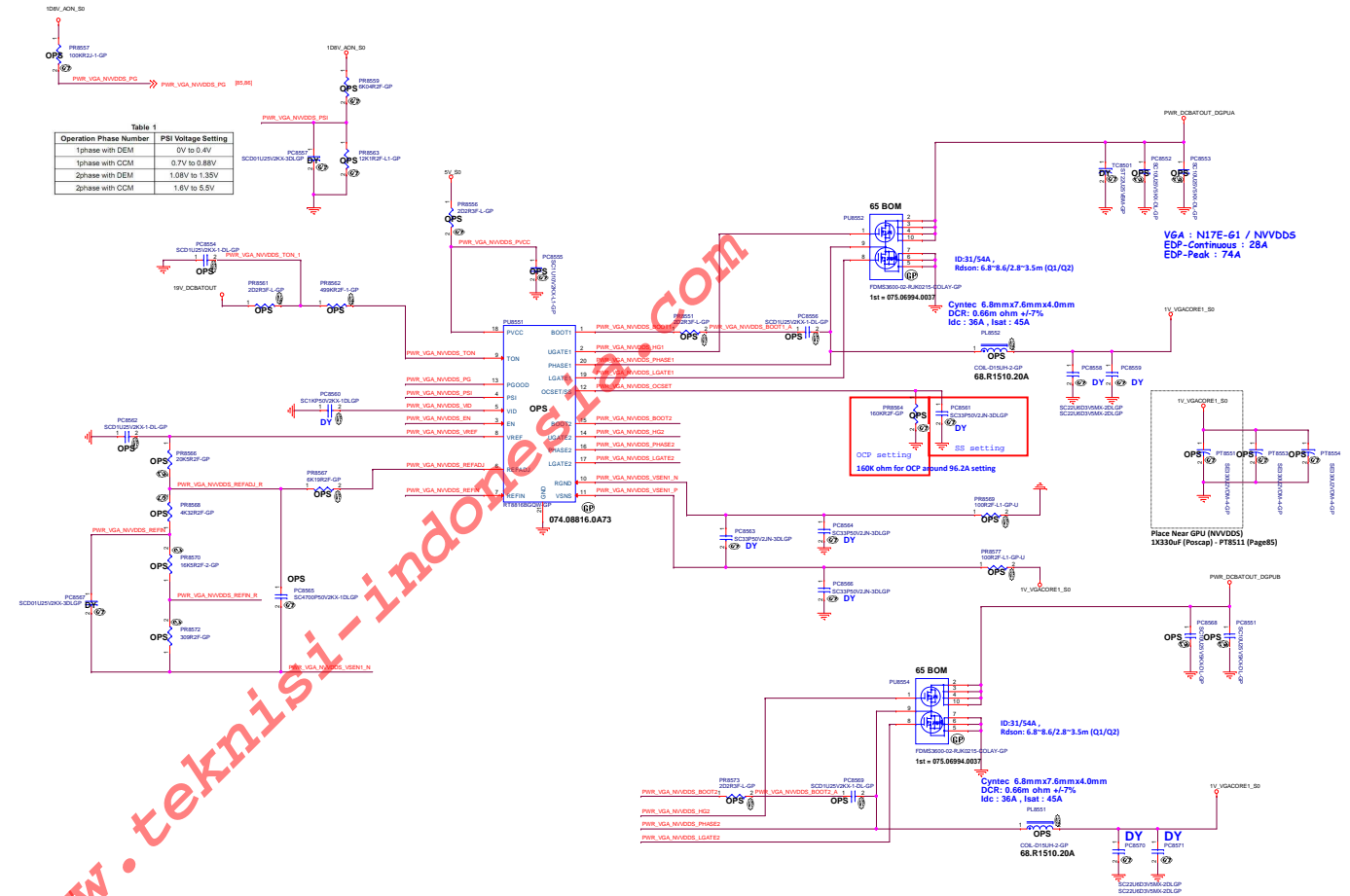
EE need check



RT8816A For NVVDDS

VGA : N17S-G1
EDP-Continuous : 30A
EDP-Peak : 60.1A


Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V



Main Func = dGPU

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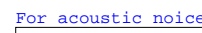
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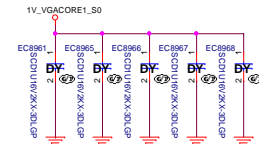
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Reserved		
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Main Func = UnusedParts



Main Func = EMI Capacitors

Mind the voltage rating of the caps.



Main Func = RF Capacitors

Mind the voltage rating of the caps.




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Main Func = TPM

[17,61,63,66,76] PLT_RST# >>>>

[18,25] SPI_CLK_ROM >>>>

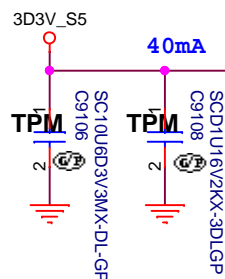
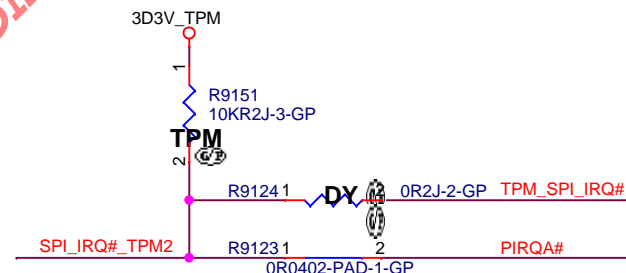
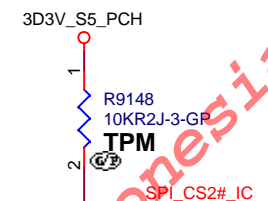
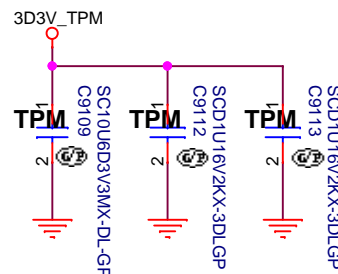
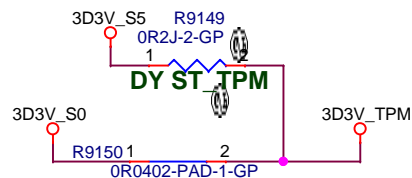
[15,18,25] SPI_SI_ROM >>>>

[18,25] SPI_SO_ROM >>>>

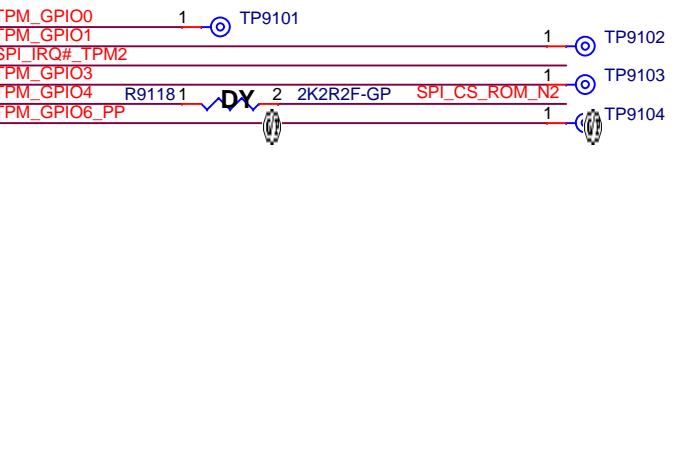
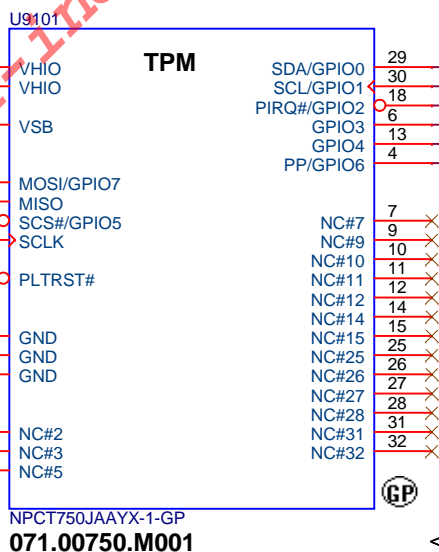
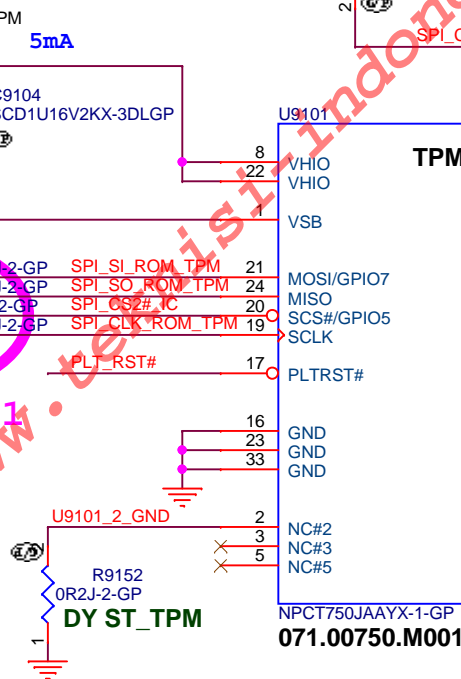
[18] SPI_CS_ROM_N2 >>>>

[20] PIRQA# >>>>

[18] TPM_SPI_IRQ# >>>>



Close to U2501

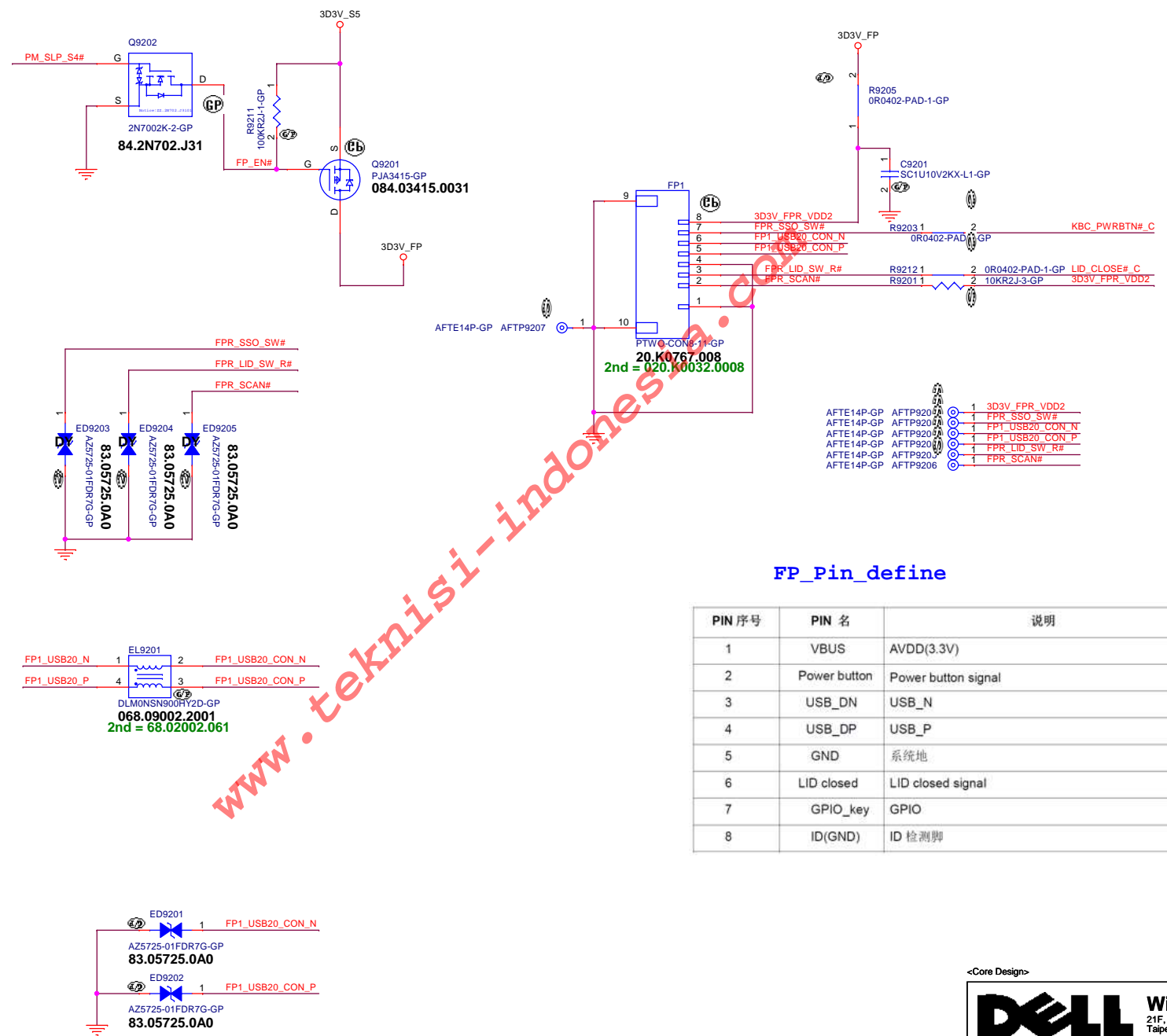


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Title INT IO (TPM)			
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SSID = Finger Print

- [24] FPR_SCAN# <<< _____
- [16] FP1_USB20_P <<>> _____
- [16] FP1_USB20_N <<>> _____
- [17,40,51] PM_SLP_S4# >>> _____
- [64,67] LID_CLOSE#_C >>> _____
- [64] KBC_PWRBTN#_C >>> _____



FP_Pin_define

PIN 序号	PIN 名	说明
1	VBUS	AVDD(3.3V)
2	Power button	Power button signal
3	USB_DN	USB_N
4	USB_DP	USB_P
5	GND	系统地
6	LID closed	LID closed signal
7	GPIO_key	GPIO
8	ID(GND)	ID 检测脚

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Title: **Finger Print**

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LVDS Switch

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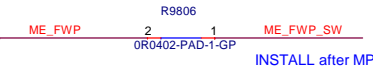
A00

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Main Func = Firmware SW

[19] ME_FWP_SW>>>
[24] ME_FWP <<<



Firmware SW


Default setting:pull LOW
DY for MP

	3	1
	LOW	HIGH
ME_FWP	Normal Operation (Default)	Override

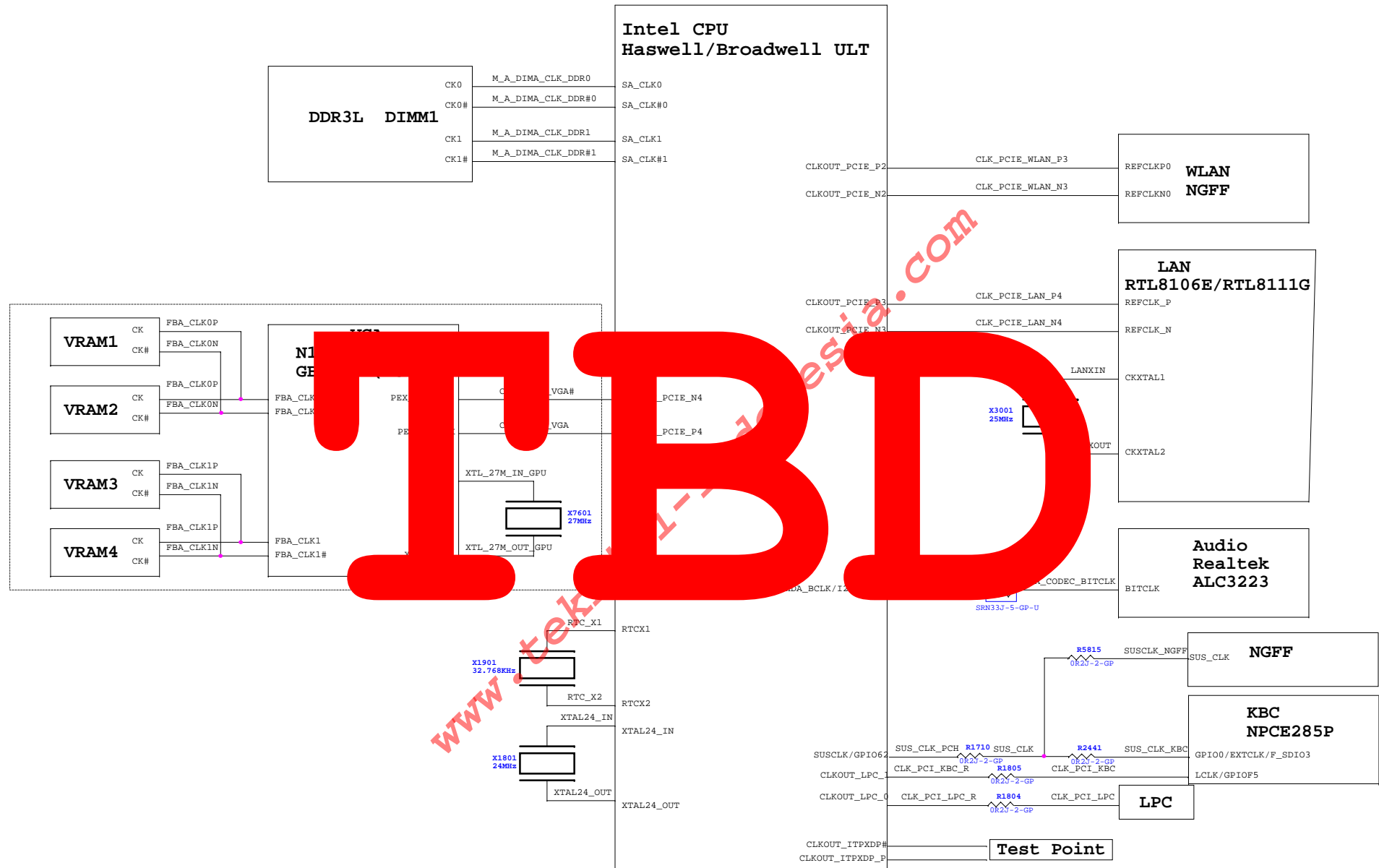
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Title Debug (XDP debug)			
Size A4	Document Number Mantis_CML		Rev A00
Date: Tuesday, May 28, 2019		Sheet 99 of	105

CLK Block Diagram



Change notes -

[illegible]

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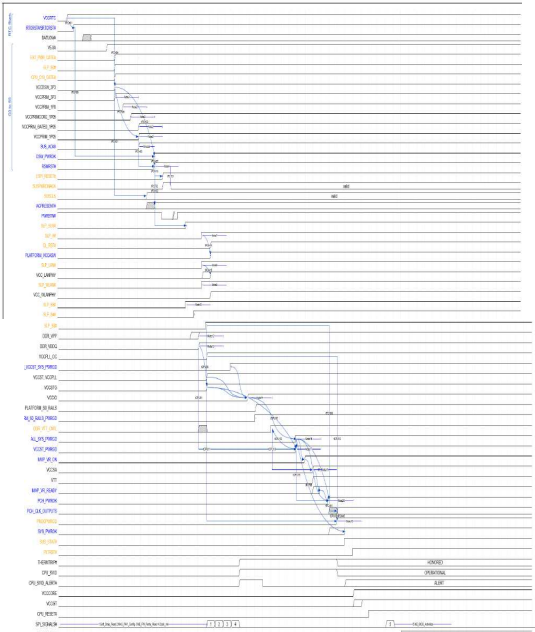
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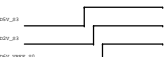
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Sheet	101	of	105
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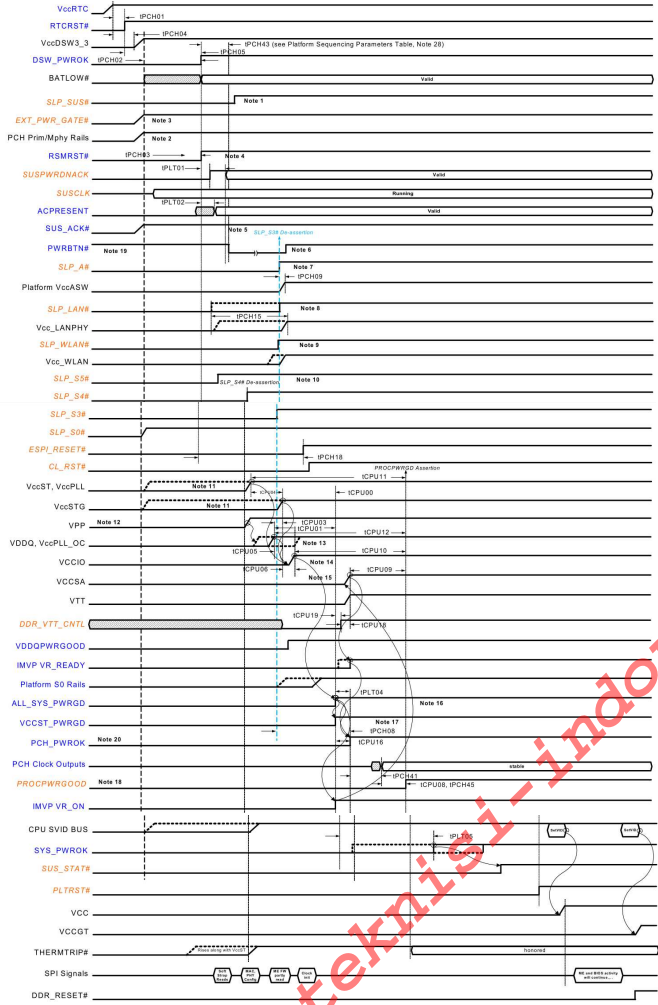
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



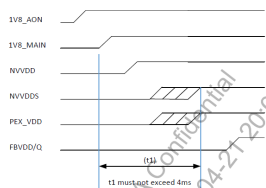
For DDR4 power sequence



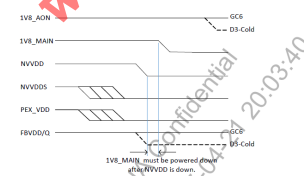
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



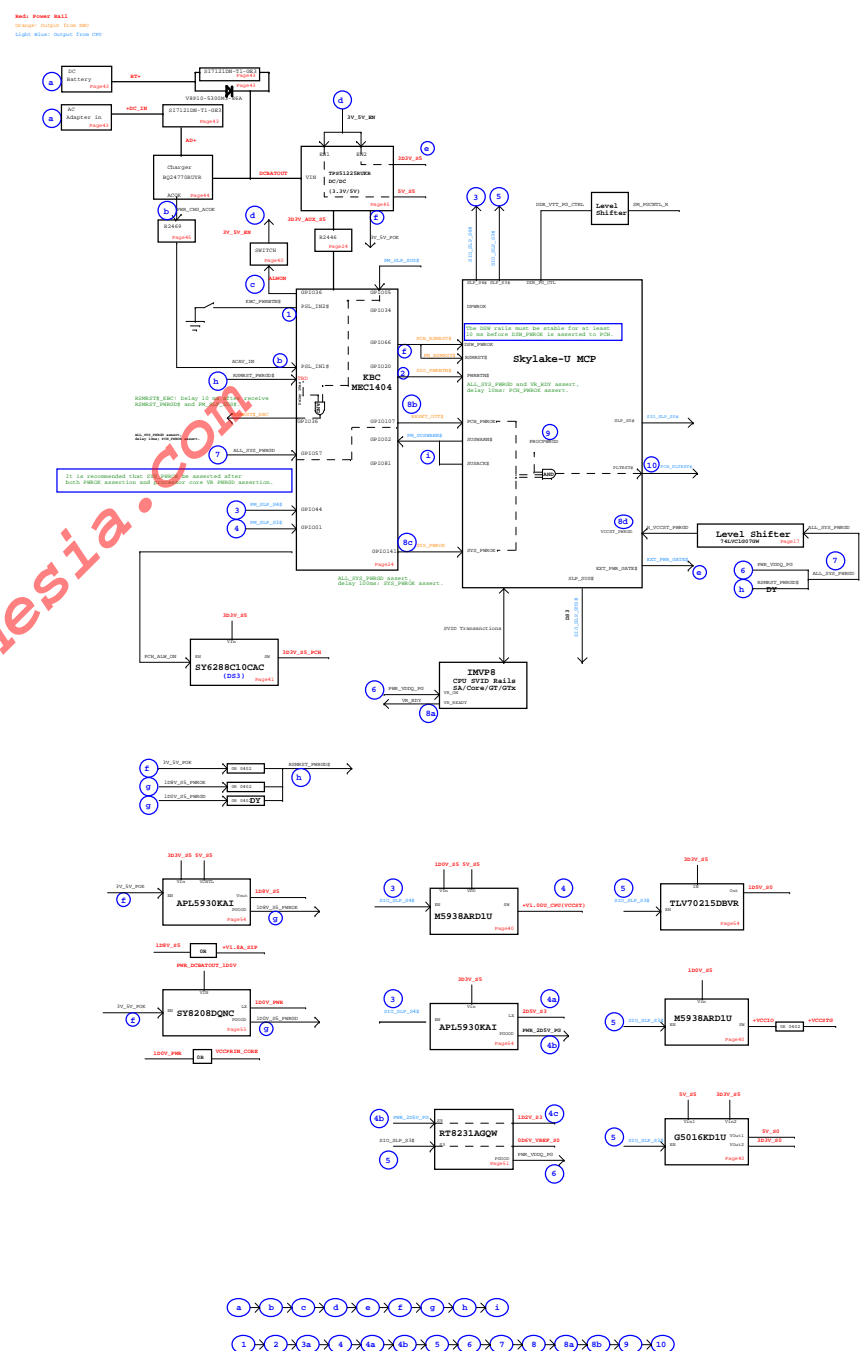
NV N17S GPU Power ON sequence

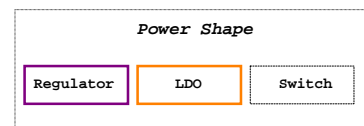
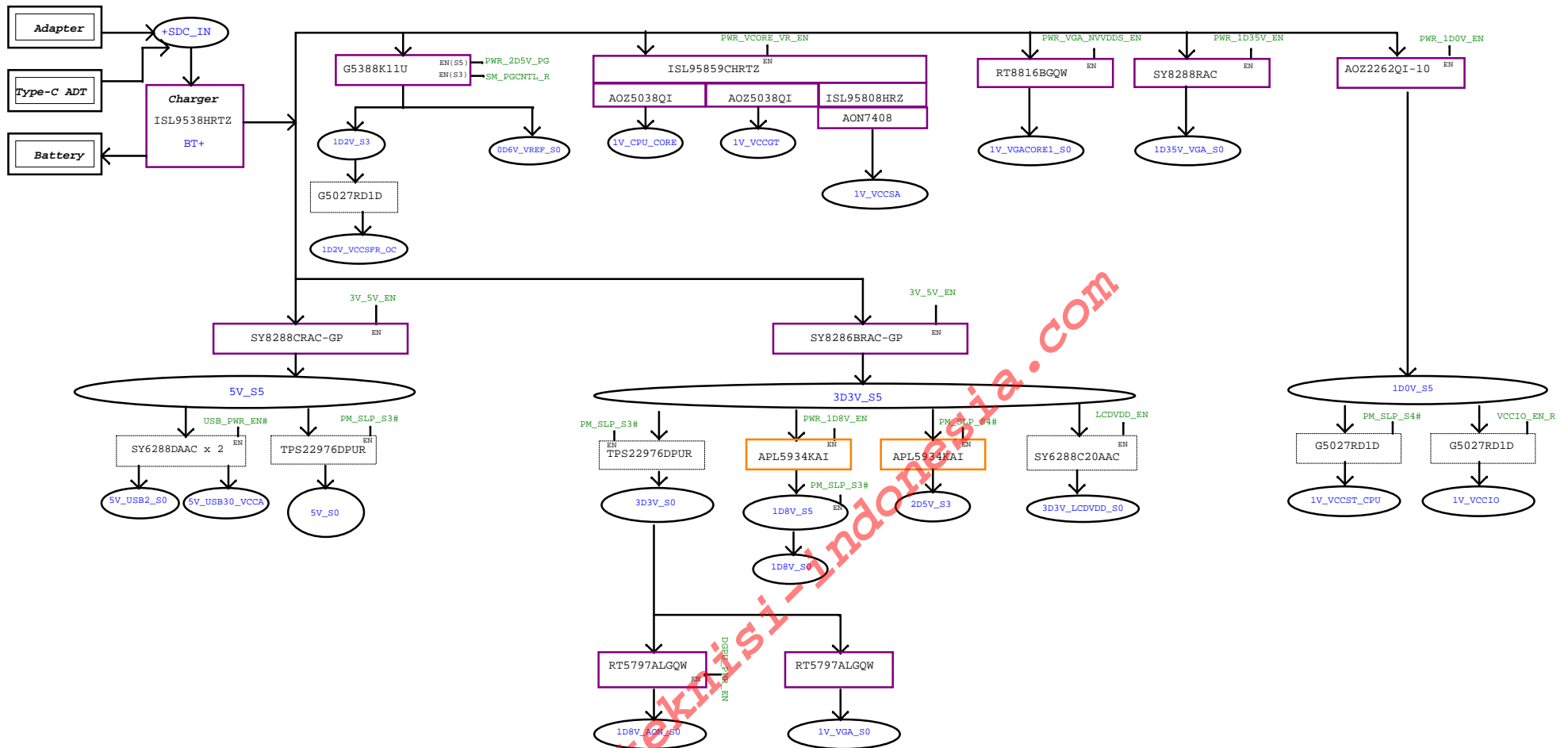


NV N17S GPU Power Down sequence

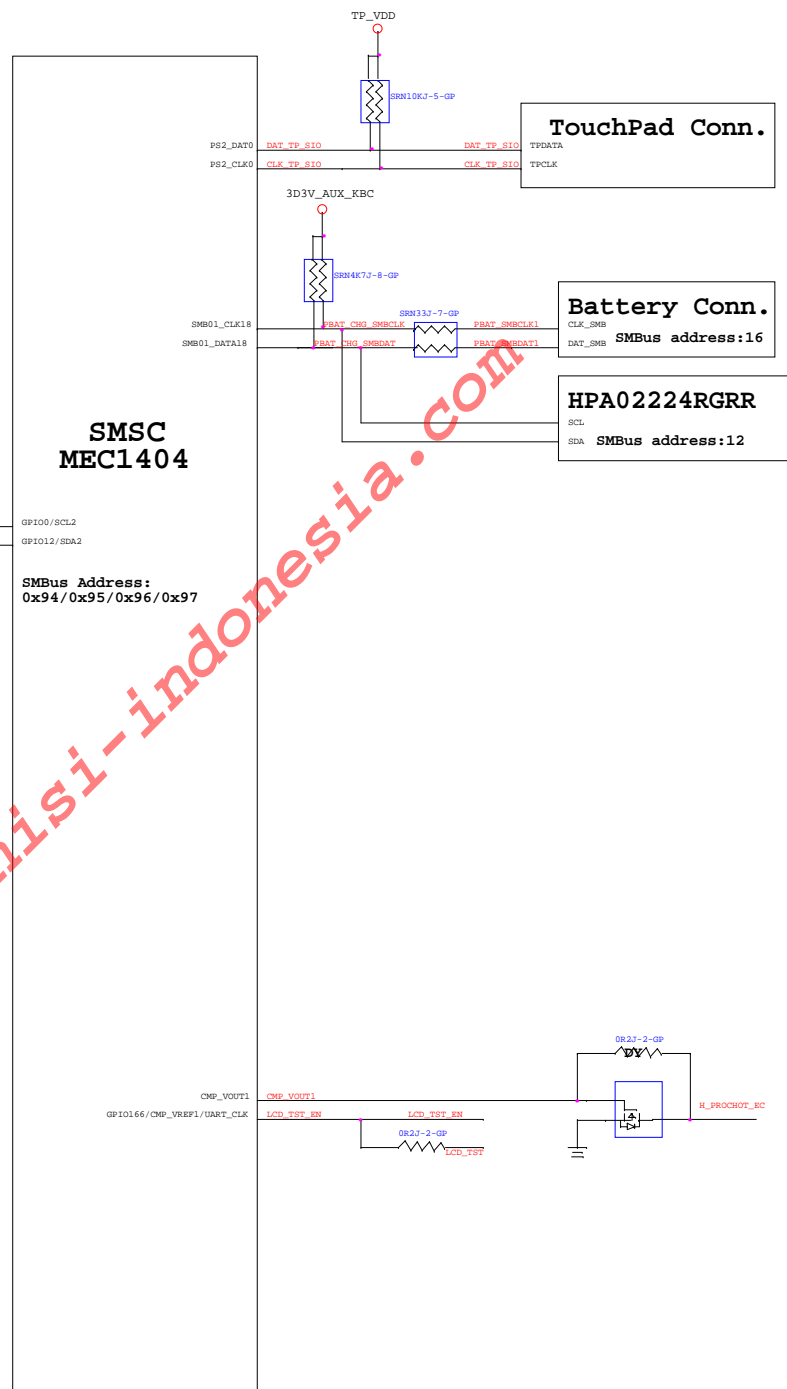


Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

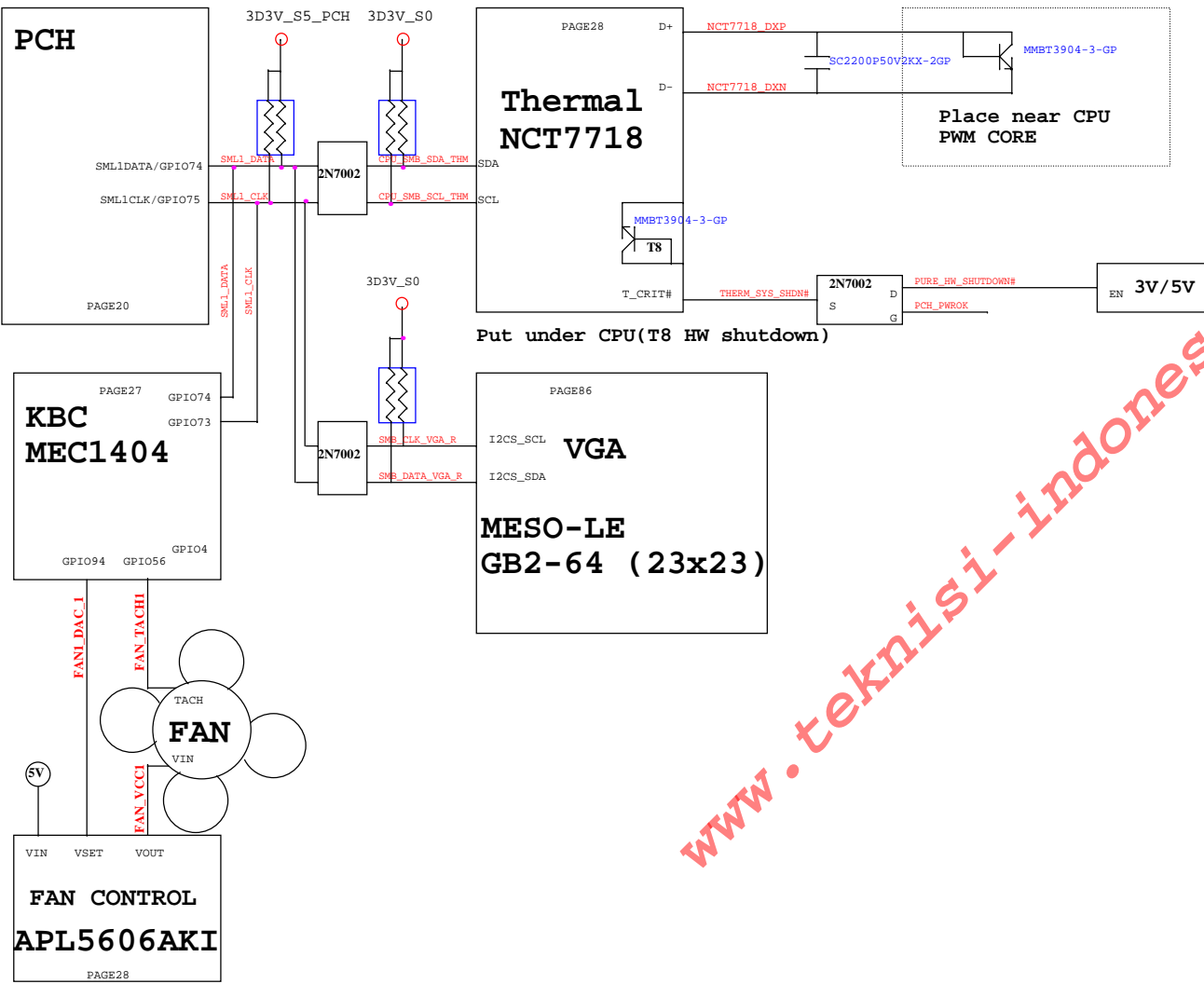




KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

